Integrated Power-Line and Visible-Light Communications

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***Abstract*—The current state of the world places an important role on communication, specifically the different mediums for communication and how we can exploit them. The issue with such mediums is that very often, there are clear disadvantages that cause them to become less viable in certain conditions. For this project, an existing VLC (Visible Light Communication) device has shown to produce high speed communications across an unblocked path of visible light. The motivation for this project stems from the fact that although a VLC device has clear advantages such as a lack of consideration of frequency bands, non licensed communication and a lack of interruption from other sources, there are clear disadvantages as well. Specifically, the datastream is extremely sensitive to external light sources, and a direct line of unblocked site is required for communication. This project calls for an addition to be made in the form of a PLC (powerline communication) device in order to act as a complementary form of communication. PLC devices do not have the advantages of license and band free communication, however they are resilient to light interference, and can operate in any conditions with a mains line by modulating, injecting, and demodulating data over said mains. This report details the development and more importantly results of the project, displaying data on several metrics of the filter system, as well as an emphasis on the development process and results of the PCB and device itself. Shortcomings and alternative results of the project are also discussed in place of metrics and results in the cases that said metrics and results could not be achieved or measured.**

I. Introduction

Communication in the digital age revolves around portraying digital data over various mediums of communication. These consist of electricity, radio waves, and more importantly to this paper light waves. VLC (Visible Light Communication) systems revolve around communicating digital data (usually binary) over some state manipulation (usually on and off states) of light waves in the visible frequency range. The advantage to such a system is of multiple layers. The main advantages the system has over more traditional communication modes, particularly radio frequencies, is that visible light does not have mandated frequency bands or licenses. Additionally, the use of a new communication medium mitigates any interference from noise via radio frequencies. A particular advantage over non visible light communication systems (infrared systems, typically found in television remotes) is that existing light sources such as home lighting systems can be repurposed to allow communication between receivers. VLC systems however, have the major disadvantage of not being able to function without a direct line of physical sight between transceiver and receiver. With this in mind, communication in busy areas with many people possibly obstructing line of sight becomes difficult, and long range communication becomes impossible. With this in mind, adding an additional communication protocol to the communication stack becomes an appealing solution, as a system that perhaps excels in the areas where VLC systems do not will allow for a more robust communication stack. The solution to this problem is envisioned as a PLC (Powerline Communication) system. PLC systems involve modulating a data signal to a specific scheme, injecting it at a high frequency onto a coupled 50/60Hz AC mains line, decoupling this signal from the low frequency line, and demodulating it back into binary data. The system is typically used either in buildings to communicate across AC mains lines, or in long range situations to allow smart metering from power distributors via PLC over long range power transmission tower lines. The disadvantages to PLC systems typically lie in sensitivity to a noise heavy environment, high costs of discrete components, and a limit on transmission speed that is usually a trade off to noise mitigation. However the advantages lie in the fact that this communication medium can be set up in any environment with an already set up power infrastructure, essentially "re-using" an existing set of electric cable for multi purpose. Additionally, PLC systems do not require a line of sight to communicate. For these reasons, a PLC system was chosen to be the accompanying system to the VLC communication stack.

Evaluation of the project by the project finish date proved that the resulting artefacts were not sufficient to be able to act as a fully functioning PLC system. The filter system devised although functional, likely requires multiple adjustments for full efficient operation, and the developed PCB for the project is currently unable of executing any code or operations. The evaluations performed on the system at hand have shown that the system is possible to be developed into a fully functioning system, and is capable of transmission up to great deals of length. Additionally, the PCB itself has been deemed to have no immediately glaring faults, and has safe readings at various points of the board.

The goal of this PLC project was to create a self contained, line powered PLC system that is capable of transmitting up to a 150 character string in well under a second. The system had to be bidirectional, be able to send messages with little to no error up to 10 meters (ideally more, up to around 50 meters), have a low power consumption to adhere to sustainability goals, and have its own enclosed housing.

This project was supervised by Yau Hee Kho

II. Related Work

Upon further inspection of the problem at hand, it is found that there are a number of alternatives to a PLC system to accompany the VLC system. In particular, the main alternatives to PLC systems are radio frequencies (both shortwave and longwave), simple wired communication and other light based communication such as infrared.

A. Digital Radio Frequency Communication

Simple wireless radio communication is a communication scheme that has been active in our world for many decades. As this project is of digital communication, the specific type of communication discussed for radio frequencies is digital radio. In terms of the data transmission scheme, digital radio is extremely similar to PLC systems, in that data is modulated under a specific scheme, sent via the transmission medium, and received to be demodulated into binary data [1], the main difference between RF and PLC is that of the communication medium. PLC systems inject the high frequency modulated data to reside inside a lower frequency high voltage mains supply. RF systems instead transmit the modulated data via electromagnetic waves that are carried airborne. A radio antenna is a specifically designed object of metal, that when subjected to small electrical currents oscillates to produce electromagnetic waves. By using the modulated data signal as this electrical current, the data signal is transmitted into free air and can travel for multiple miles before dying out. Transversely, the same type of antenna will produce the same electrical current when subjected to electromagnetic waves. The electrical current produced can then be decoded into the original binary data, completing the transmission and receiving. Digital radios, being a wireless communication protocol, are capable of transmitting and receiving data from any two locations within it's operational boundaries. As such, it could be argued that an RF system may be a better choice as a complimentary system to the VLC system. However, it is important to realise that RF systems have a number of substantial downsides when compared to PLC systems. In particular, as radio systems have been operational for decades, the radio frequency spectrum is increasingly congested with a large range of commercial and personal radio systems. Although PLC systems do suffer some congestion in the form of smart metering applications from power companies in the form of CENELEC bands, the interference risk is far lower, and the range of frequency bands far more vast than that of radio systems. Additionally, as one of the main advantages of a VLC system is that it can operate freely in areas of high radio interference or poor radio performance, it does not make logical sense to oppose this distinct advantage of the system by introducing a wireless radio communication system. Thus, a PLC system offers a better solution when it comes to highlighting the advantages of a VLC system, while diminishing the disadvantages of the same system.

B. Wired Conductor Communication

In the absence of an AC line, a simple replacement is wired communication. Usually, this is done via some sort of communication scheme such as SPI, I2C etc. To simplify, communication in this fashion is the process of sending binary data through specifically timed electrical impulses via a conducting wire. The advantage of this simple scheme lies in its simplicity, schemes such as UART can be set up with as little as a transmit and receive conductor, and offer reliable high speeds up to the 4Mbps (Megabits per second) mark [2]. The main disadvantage of course, is in the fact that such a scheme disregards the purpose of adding another communication protocol to the stack. The VLC system is capable of being set up in any location the user desires quickly and efficiently, with the major drawback being that it requires a direct line of sight. A PLC system also has the advantage of being quick and easy to set up in practically any environment (given a mains line), however a conductor based setup does not have this advantage and would need to be set up using conductor routing. Additionally, a conductor approach typically will not be able to communicate for long distances without some form of repeater, while a PLC system typically is capable of long range communication given a strong medium (mains line). For these reasons, a wired conductor would not be suitable as a complimentary communication system.

C. Infrared Communication

Infrared communication is extremely similar to visible light communication. In particular, it simply replaces the visible light aspect of a VLC system with infrared light, which is at a frequency not visible to the human eye [3]. There is very little difference between the two schemes in terms of data rate, function and use cases. The main difference is that VLC systems can repurpose already existing infrastructure (existing light sources) for communication in a similar fashion to PLC systems (existing mains infrastructure). For these reasons, it does not make sense from a system level standpoint to implement infrared as a complimentary communication system.

III. Design

The design process for the system level overview involved chosing not only a system scheme/layout, but also defining and refining various specifications and restrictions that the project must adhere to.

A. System Level Scheme Design

Initially, the overall setup for the PLC system had to be considered. In majority of existing PLC systems, the system setup consists of a PLC modem, a filter system, some sort of microcontroller, and other discrete hardware for various other purposes. It is possible however to create a more direct approach, in which the high frequency data signal is modulated and sent via a microcontroller and tone generators, and filtered out on the opposing side via filters and the microcontroller. This approach has the advantage of being cheaper and more direct, as well as taking up less physical space on a PCB. The disadvantage however, is the fact that such a setup is limited to what you build it for. If you want to change any aspects of the

system such as data rate, modulation scheme, or anything else, it requires a board redesign. It is also lacking in feature sets, as you are limited in operation to whatever a microcontroller and tone generators can achieve. With this in mind, the traditional setup of a PLC modem, a microcontroller, a filter system and a set of discrete components was chosen mainly for a more robust, and feature rich system. Fig. 1 and Fig. 2 display the initial scheme and the chosen scheme respectively.

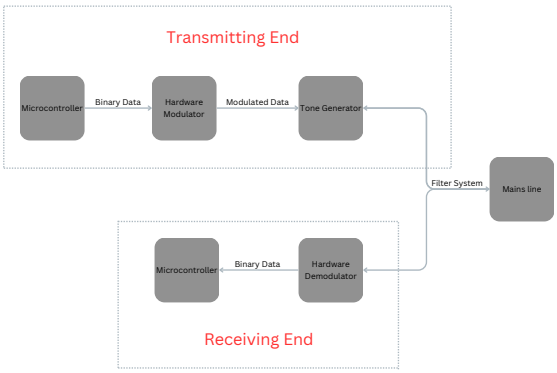

Fig. 1. **Initial Considered PLC System Level Design**

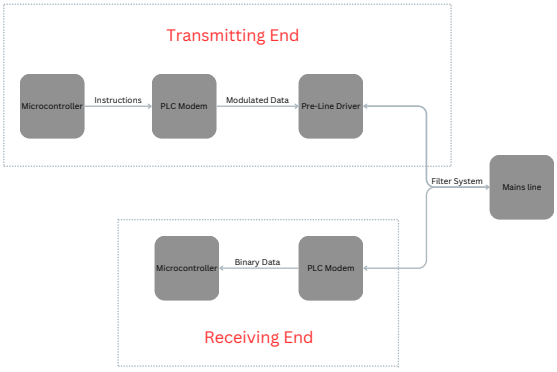

Fig. 2. **Modernised Chosen PLC System Level Design**

B. Frequency and Band Restrictions

Another consideration to make was the frequency and band scheme. Typically in PLC systems, any transmission/receiving frequency above 500KHz is considered broadband, and anything below is considered narrowband. Typically, broadband PLC systems allow for higher theoretical data rates at the expense of possible distance and an increased BER (Bit Error Rate). Narrowband systems offer longer possible distances and lower inherent error with the tradeoff of lower possible data rates. In referencing the specification defined earlier that the system must be able to transmit a 150 character message in under a second, an informed decision can be made. A single UTF-8 character is 8 bits, making a 150 character message approximately 1200 bits. When it is considered that the modern narrowband PLC modems are capable of up to 32kbps under the G3-PLC standard [4], it is realised that this allows a narrowband system to send this message in 0.04 seconds. With this in mind, and that a large transmit and receive distance is another specification required, a narrowband system is the best possible solution to leverage the advantages of said system while minimising the disadvantages.

When considering a frequency with which to transmit and receive, the initial limitation was that of a narrowband system having a frequency below 500KHz. With this in mind, although the project was to run on a stepped down 12V 50Hz AC mans signal replacement, the next consideration that would allow the system to possibly in the future be modified for real mains use was that of governed standards on frequency bands. In New Zealand, CENELEC bands are used by power companies and other companies that use PLC systems. As a result, any frequency modulated and injected onto a mains line between 0 and 148.5KHz is either prohibited or monitored with extreme conditions [4]. A frequency of 240KHz for transmit and receive was chosen, as it falls into the safe zone while still being a narrowband transmission.

C. Filter Topology Design

Following on from this decision, was the decision on a filter topology. Typically in a PLC system, there are two or three filter systems split up into various categories [5]. There is usually both a transmit and receive filter. For a transmission filter, the input is the 240KHz data signal, and the output is the same signal with any excessively high noise (¿ 500KHz) filtered out, as such this filter is usually a bandpass filter. For the receiving filter the input is the 50Hz AC mains with the 240KHz data signal injected on top. The output must simply be the 240KHz signal to be demodulated, therefore the 50Hz signal must be filtered out. For this reason the receiving filter is typically either a high pass filter that blocks 50Hz but allows 240KHz, or a band pass filter that passes frequencies in the range of 230-250KHz. Additionally, a filter can be introduced that doubles as a coupling system. This filter for simplicity and convenience sakes can be configured the same way as the receiving filter to further filter out both excessively high and low frequencies. It is a requirement for this filter to be of some form of LCR configuration, as the capacitor in the filter is required to successfully couple the high frequency signal to the mains line. The typical 3 filter topology was chosen for each side of the system, for a total of 6 dedicated filters to the system, 2 receiving, 2 coupling and 2 transmitting. These were chosen to be passive filters for several reasons. The main reason is that as the frequency in question in a filter becomes higher and higher, an active (op amp based) filter design requires an op amp that is capable of processing high frequency signals (these can be increasingly expensive). Passive filters also save on component cost, PCB space, and have guaranteed stability. For these reasons, all 6 filters were intended to be passive filters. Fig. 3 shows a flow chart of the envisioned filter system(s).

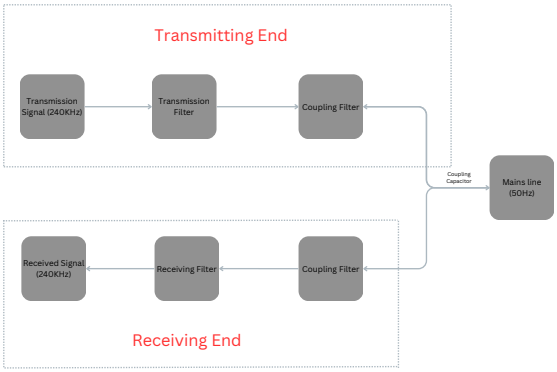

Fig. 3. **Chosen Filter Topology**

D. Gain Considerations

An important factor to consider with PLC systems is gain. When injecting a signal of fairly low voltage (3V) to a line with higher voltage and far higher current (12V at 105W), it is inevitable that the sheer size difference in voltage and current can result in the injected signal being diminished. Additionally, the use of passive filters often provide gain that is either only 1 (ideally), or often less than 1, causing the voltage levels of the output signal to be smaller than the input signal. PLC modems often have built in gain amplifiers on the receiving end to amplify the received signal to an appropriate voltage level, however this alone is often not sufficient for clean data to be received. As such, some sort of pre-transmission amplifier was chosen to be part of the overall system design. This amplifier is responsible for amplifying the transmission signal to a higher voltage level so that it does not get "lost" in the mains line.

E. Discrete Component Tolerance Restrictions

The simple choice to prioritise tolerances of discrete components was made in the late stages of development, with the caveat that these parts be within reasonable limits given increased costs of low tolerance parts. This was especially relevant for the filter system, in which small variations from the simulated/theoretical values can cause large variations in the filter's operation and output characteristics. As such, the goal was set for discrete components to have a maximum tolerance of 1%, with increases beyond that deemed acceptable if it resulted in lower system costs (the low tolerance part being exceedingly expensive).

F. Sustainability and Safety Restrictions

The final two design requirements were that of sustainability and safety. In order to ensure safety, the typical mains line used in PLC systems (230-240V 50Hz mains AC line) was replaced with a step down converter giving an output of an AC line that is still 50Hz but of a much lower and safer 12V. Fundamentally, the only difference in designing the filter system for a 12V line over a 240V line is simply the required voltage and current ratings for inductors and capacitors within the system alike. Additionally, the design specification for the system to have a low power consumption and use ROHS compliant parts was made to adhere to sustainability standards and goals.

IV. Implementation

With the design process yielding a systems level approach, and a set of restrictions/speficications, the next stage in the project design was bringing the envisioned design into reality via implementation.

A. Filter Implementation

The design stage of this project left a set of specifications for implementing this design into a working set of filters. We are given the specifications that:

- The filters must all be passive
- There will be 3 pairs of filters, 1 pair of transmission filters, 1 pair of receiving filters and 1 pair of coupling filters
- The transmitted data signal must be of 240KHz
- The mains line is of 50Hz
- The transmission filter must filter out excessively high frequency noise
- The receiving filter must only allow the 240KHz signal to pass while blocking the 50Hz mains
- The coupling filter must have the same function as the receiving filter

With these specifications in mind, the following filter designs were implemented:

1) Transmission Filter Implementation: The transmission filter topology was decided early in implementation. As the main requirement is to pass a 240KHz filter while blocking excessively high noise and still passing low noise (as it was assumed the rest of the filter system would sufficiently deal with low noise), a filter topology with a steep attenuation would allow the least amount of noise to pass. As such, a fourth order low pass butterworth filter was envisioned. Butterworth filters are a topology of filter that have a number of distinct advantages when it comes to designing a low pass filter with a steep attenuation, and a maximally flat response in passing frequencies. Although technically there are filter schemes that can produce a steeper attenuation at the same filter order (Chebyshev filters are particularly good at this), the Butterworth filter provides a balanced tradeoff between attenuation, and a flat response in the passband [6]. The fifth order state of the filter design was chosen to double the attenuation from 20dB per decade to 40dB per decade. In the preliminary report for this project, the formula and mathematics for designing this filter were described. To reiterate, the design process for this type of filter begins by specifying a frequency at which we wish the attenuation to be of a magnitude of -3dB, as a good rule of thumb we can make this twice as large as the frequency we wish to be passing (so 480KHz). Stephen Butterworth, the designer of the butterworth filter, created a table with which to design filters with [7]. Referencing this table, we can ascertain a list of denormalisation ratios, these being 0.618, 1.618, and two

instances of 1.0 to add to 2.0. From here, the process is to find normalised values for the inductors and capacitors that build this circuit. Given the use of a fixed 1K resistor as the filter's resistor and a value for ω_{-3dB} of $2\pi 480000$, the normalised inductor value is given by:

$$L_r = \frac{R}{\omega_{-3dB}}$$

$$L_r = \frac{1000}{2pi(480000)}$$

$$L_r = 0.000331572798$$

Similarly, the normalised capacitor value is given by:

$$C_r = \frac{1}{RX\omega_{-3dB}}$$

The X component in this circuit can safely cancel to zero, giving us a calculation and value of:

$$C_r = \frac{1}{1000(2pi(480000))}$$

$$C_r = 0.000000000331572798$$

Given these values, multiplying the capacitor value by 0.618 gives values for capacitor C1, and capacitor C3. Multiplying it by 2.0 also gives us the value for C2. Multiplying the inductor value by 1.618 gives the value for both L1 and L2. These values are as follows:

$$C_1 = C_3 = 0.618(0.000000000331572798)$$

$$C_1 = C_3 = 0.000000000204911989F$$

$$C_{1real} = C_{3real} = 0.2nF$$

$$C_2 = 2.0(0.000000000331572798)$$

$$C_2 = 0.000000000663145596F$$

$$C_{2real} = 0.68nF$$

$$L_1 = L_2 = 1.618(0.000331572798)$$

$$L_1 = L_2 = 0.000536484787H$$

$$L_{1real} = L_{2real} = 0.56mH$$

As the transmission system already lets higher frequencies than 240KHz in the 300-400KHz zone pass with some attenuation, the distinct accuracy of this system is not so necessary that multiple components had to be used to sum correct values. Therefore, all capacitor and inductors were rounded in their values to the nearest E12 series standard element. An additional 1K resistor is added between the output and ground, as this was found to greatly reduce the peak gain at frequencies of around 500KHz, and created a smooth butterworth filter result.

Upon arriving at this stage, the process was to place the component values in the correct locations for this filter topology inside an LTSpice simulation. Fig. 4 shows the schematic of the transmission filter. Note the changing of component values to fit within the E12 and E24 standard array of parts, upon testing this yielded very similar results.

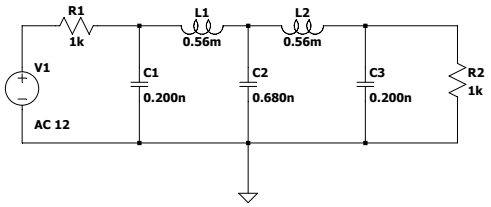

Fig. 4. **Transmission Filter Schematic**

It is noteworthy to state that the values used for components of the transmission filter vary greatly from that of the filter found in the preliminary report. This is because the transmission frequency was adjusted from 14KHz to 240KHz to comply to CENELEC standards. Additionally, the 1 ohm resistor in the original design dissipated excessive power as heat, and thus the calculations were redone with a 1K ohm resistor as shown.

2) Coupling Filter Implementation: The coupling filter had few options in how the filter could be designed. In particular, the filter must be passive, block 50Hz and other low frequency signals while passing signals in the 240KHz range. The unique requirement of the the coupling filter is that it must be bidirectional, in which it both must be able to decouple the high frequency signal from the mains line, and inject a new high frequency signal into the mains line. As a result, the only sensible filter topology is that of a series LCR band pass filter. This choice is made as an LCR band pass filter is capable of performing these main requirements in the form of a coupling capacitor. While in other filter topologies the signal can get easily lost when injected from the opposing end of the filter, the series element of the capacitor in an LCR band pass filter mitigates this issue. Additionally, series LCR filters have the characteristic of being very low impedance at resonance (i.e. at the passband), meaning that the low impedance of a mains line is more readily impedance matched to allow for a higher quality signal.

A band pass series LCR filter is mathematically fairly simple to implement. The formula for the centre frequency of a series LCR bandpass filter is given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

Additionally, the bandwidth of this filter is given by:

$$B = \frac{R}{L}$$

After choosing a standard inductor value of 4.7uH, and realising a centre frequency of 240KHz, the following calculation provides the value of the capacitor required (note that this formula is simply a rearrangement of the centre frequency formula):

$$C = \frac{1}{4\pi^2 L f_0^2}$$

$$C = \frac{1}{4\pi^2(0.0000047)(240000)^2}$$

$$C = 0.0000000935664005F$$

$$C = 0.094uF$$

With an inductance chosen, usually the process is to choose a desired bandwidth and then calculate the required resistor value for such a bandwidth. Unfortunately, testing desired bandwidths produced a power draw in the resistor that was far from sustainable. As a result, an arbitrary value of 100 was chosen for the resistor. While this unfortunately changed the bandwidth so greatly that the band pass filter now operated like a high pass filter, this was a compromise that had to be made. The saving grace of this process is that not only does the receiving filter properly operate as a band pass filter at the correct frequency, but the coupling filter is still successful in blocking low frequency (50Hz) signals. The resulting schematic of this filter is shown in Fig. 5.

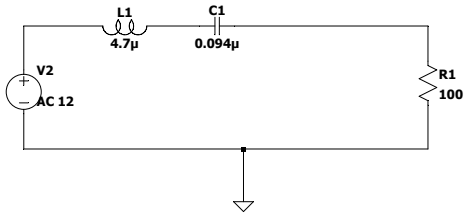

Fig. 5. **Coupling Filter Schematic**

Again, the values for the filter differ from those of the preliminary report. This is again because of the change of transmission signal frequency, as well as because of the adjustment of the high power consumption 1.2 ohm resistor to a more reasonable 10K ohm resistor.

3) Receiving Filter Implementation: The receiving filter simply had to be some filter topology with the same band pass specifications as the coupling filter. As such, simply taking the series LCR band pass filter and altering it into a parallel LCR band pass filter is sufficient for the filter operation. At resonance (passband), the impedance of a parallel filter is high, this high impedance is effective at both rejecting excessive noise still present, and passing desired frequencies with far less attenuation.

The underlying mathematics for a parallel LCR band pass filter is similar to that of the series filter. The formula for the centre frequency of the filter is again given by:

$$f_0 = \frac{1}{2\pi\sqrt{LC}}$$

However, this time differing, the formula for the bandwidth of the filter is given by:

$$B = \frac{1}{RC}$$

By choosing an inductor value of 1mH, and again realising a centre frequency of 240KHz, the following calculation provides the required capacitor value.

$$C = \frac{1}{4\pi^2 L f_0^2}$$

$$C = \frac{1}{4\pi^2(0.001)(240000)^2}$$

$$C = 0.000000000439762083F$$

$$C = 0.44nF$$

Unlike the series filter, the bandwidth formula was properly used for this filter. By specifying a bandwidth value of 12727 and performing the following calculations, we realise a resistor value:

$$12727 = \frac{1}{R(0.00000000044)}$$

$$R = 178570\Omega$$

Upon constructing this filter in LTSpice, Fig. 6 displays the filter schematic

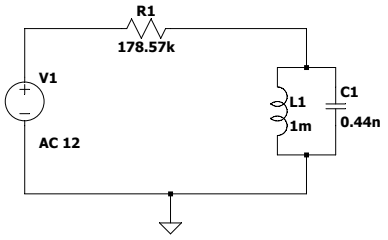

Fig. 6. **Receiving Filter Schematic**

Finally, the receiving filter aswell has different component values to that of the preliminary report. This is once more because of both the change in transmission frequency, and resistor value.

B. Filter System Component Selection

The filter system required a detailed component selection process, as the system is meant to deal with precise high and low frequency signals. Large deviations between real components (due to tolerances) and simulated components can lead to undesirable filter operation. Additionally, the type of capacitors chosen for the filters was of equal importance, as certain types of capacitors can have undesirable parasitic effects such as inductance and resistance, as well as certain types of capacitors having a better frequency response at high frequencies. The final filter design consisted of capacitors, inductors, resistors, and an isolation transformer (which was discarded).

1) Capacitor Selection: Capacitor selection was perhaps the most intricate component of implementing the filter design. In terms of capacitor types, there are many different physical solutions to creating capacitance that come in the form of different capacitor designs. The two most common capacitor types are electrolytic capacitors, and ceramic capacitors. Electrolytic capacitors are known for being cheap for large capacitance, with the downsides of high tolerance, poor frequency response at high frequencies, strictly polarised operation and high parasitic inductance and capacitance. Alternatively, ceramic capacitors have poor capacitance for higher prices, while instead maintaining low parasitic values, good frequency response at high frequencies and no requirement for polarised design. Due to the bidirectional nature of the coupling filter, ceramic capacitors were the first major consideration for this implementation. However, there are capacitors that theoretically perform even better in all regards when compared to ceramic capacitors.

Film capacitors are known typically for their large list of advantages over traditional capacitors. While the limits of capacitance values are largely similar to that of ceramic capacitors, film capacitors are also non polarised and boast an impressively long shelf life. In particular PP (PolyPropylene) film capacitors are known for their role in high frequency applications. This is because their strong dielectric constant and low loss factor are scarcely dependent on operating frequency [8]. For these reasons, it was deemed logical to use PP film capacitors for all the filters in the filter system. For capacitance values that were not standard E12 or E24 series values, the closest possible values were formed by using two PP film capacitors in parallel.

2) Inductor Selection: Inductor selection was far more simple. There are not typically types of inductors that are specialised for specific applications. Therefore, the only requirements for each inductor was that the rated current be sufficient for the operation. As such, standard cheap inductors were chosen.

3) Resistor Selection: Resistor selection was performed exclusively on the basis of minimising error in the resistor values. As such, all resistors for the filter system were chosen to have 1% tolerances or lower, with the exception being the instances where this proved to be expensive.

4) Vera Board Use: All the filters were assembled on strips of vera board. This was done because of the implicit purpose of the developer board being to develop a rough but working system, and then use that system to develop a finalised board.

C. Filter System Assembly

Assembly was simple. The transmission filter was assembled on its own piece of vera board, after assembling each individual component, the pair of filters can be seen in Fig. 7.

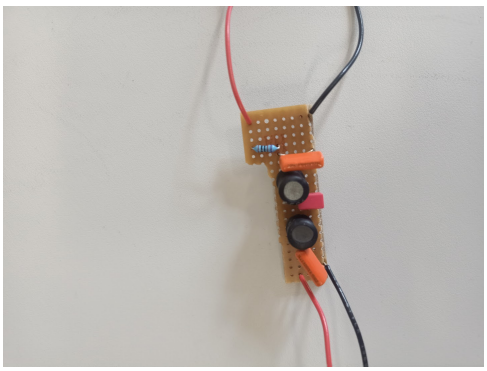

Fig. 7. **Physical Transmission Filter Implementation**

The receiving and coupling filter were assembled on the same vera board, an extra wire was included were the injected data signal will flow to. The pair of these filters are seen in Fig. 8.

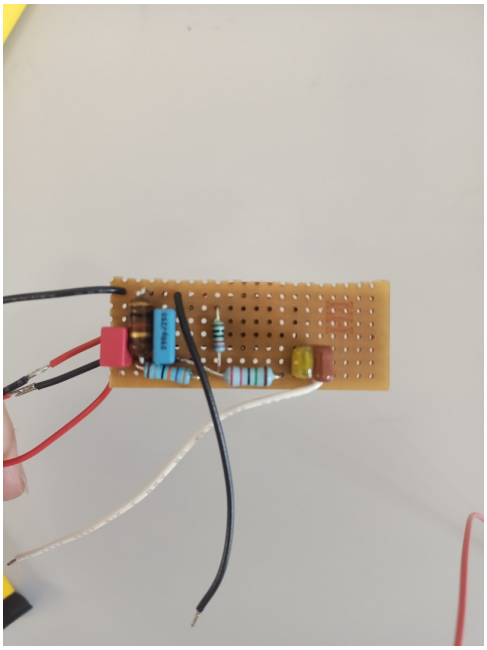

Fig. 8. **Physical Receiving and Coupling Filter Implementations**

D. Component Selection + Design Implementation For Development Board PCB

After the filter system was designed, component selection for the PCB was the next stage of implementation. A PLC

modem and preline driver had to be decided on, as well as various components for proper operation of the main PCB.

1) PLC Modem Selection: Component selection quickly proved to be not only a large amount of work, but extremely complicated. The earliest instance of component selection was in choosing a PLC modem. Initially, the ST7540 by STMicroelectronics was considered due to its reasonable cost, and simple implementation scheme. It is a half duplex, frequency shift keying only PLC modem, with the main disadvantage being that its release date (2006) puts it at risk of being discontinued in following years. Although having a simple and intuitive implementation, it is lacking in some features such as a DAC (Digital to Analogue Converter), a built in front end microcontroller, and various GPIO pins. With this in mind, the ST8500 was chosen in its place. The ST8500 again by STMicroelectronics is a 54 pin QFN packaged PLC modem that contains both a back end "real time engine", a front end ARM Cortex M4F CPU (microcontroller), dedicated SRAM (Static Random Access Memory), PGA (Programmable Gain Amplifier) and a selection of communication protocols such as I2C (Integrated Integrated Circuit), SPI (Serial Peripheral Interface) and UART (Universal Asynchronous Receiver-Transmitter). In addition, the chip has a large selection of GPIO (General Purpose Input and Output) pins that can be configured for many use cases such as specifying boot sources, communicating via communication protocols, and being configured to pulse high or low as general inputs or outputs. The ST8500 is capable of modulating and demodulating signals of up to 500KHz in frequency, and as a narrowband PLC modem is typically designed for long distance operation. Additionally, the chip is low power, ROHS compliant, and was released within the past 3 years ensuring that the chip will not be discontinued in the near to distant future. For these reasons, the possible disadvantage of a higher complexity level was chosen to be a suitable tradeoff for a suite of new and useful features, and the ST8500 was chosen early in development.

2) ST8500 1.1V Regulator Selection/Process: The ST8500 has a specific design requirement that must be fulfilled by an additional component. The modem requires a 3.3V power signal, a 2.2V, and a 1.1V. Internally, a voltage regulator produces the 2.2V signal, however the 1.1V signal must be externally supplied. Fortunately, STMicroelectronics produces a small 3.3V to 1.1V voltage regulator that with the aid of some discrete components produces the desired 1.1V power signal. The datasheet [9] specifies the requirement of an input and output capacitor, of which values 4.7uF and 22uF were chosen respectively. A 2.2uH inductor is also specified as a fixed required value inductor. A voltage divider is also specified in order to tune the output voltage. The output voltage is given by the following equation:

$$V_O = V_{FB}(1 + \frac{R_1}{R_2})$$

V_{FB} is the feedback voltage and is specified to be 0.6V, therefore in order to achieve the desired 1.1V value, the value of $(1 + R_1/R_2)$ must be equal to 1.8333. An R1 resistor of 10K was chosen and an R2 resistor of 12k was chosen. The schematic for this small regulator component of the system can be seen in Fig. 9. Tight tolerances for the capacitors were not required, so two standard electrolytic capacitors were chosen with voltage ratings of 50V and 63V respective. The value of the resistors in the divider however did require tight tolerances as deviations in the resistor values would give an undesirable voltage level. In a project dealing with a higher voltage level this difference would be negligible, but for hardware that requires low voltage inputs even the slightest deviation can cause undesirable results. As a result, two 1% tolerance resistors were chosen.

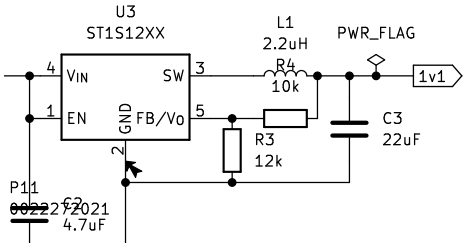

Fig. 9. **1.1V Voltage Regulator Schematic**

Additionally, the specifications of both SPI and I2C require several resistors. Typically, SPI and I2C require low ohmage resistors (in the range of 10-500 ohms) in order to operate. I2C also requires pull up resistors in order for the system to have a clear definition of what is "high" and what is "low", for this 4.7K ohm resistors are sufficient. These resistors were all chosen to have tolerances of 1% simply to narrow down possible issues arising. The resistors and communication ports are shown in Fig. 10.

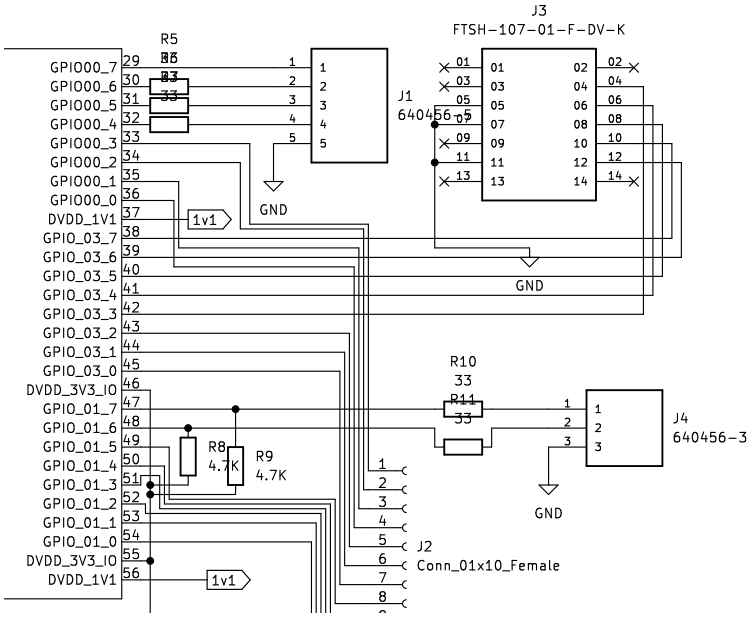

Fig. 10. **Communication Ports and Resistors Schematic**

3) Pre-Line Driver/Amplifier Selection: The ST8500 is designed by STMicroelectronics, who also design and produce a large range of other electronic components and ICs. As such,

STMicroelectronics actually produces a pre line driver that is not only suitable for pre line amplification with the ST8500, but actually specifically designed for operation with it [10]. The STLD1 is a pre line driver IC produced by STMicroelectronics. It is a dual line driver meaning that although for the purposes of this project only one line is required, it is capable of transmitting differential signals [11]. It is capable of amplifying a signal to up to 1.5A, and 18V. As it is designed for the ST8500, there was no reason not to choose this component as the preline driver. The IC specifically does not require any discrete hardware to operate, just the correct connections. The exception to this, is a single 10uF capacitor between the 5V output supply and the 0th reserved pin. Tight tolerances are not required for this component, so a standard 20% 10uF 200V capacitor was chosen. Fig. 11 displays the schematic for the STLD1 pre line driver component of the system schematic.

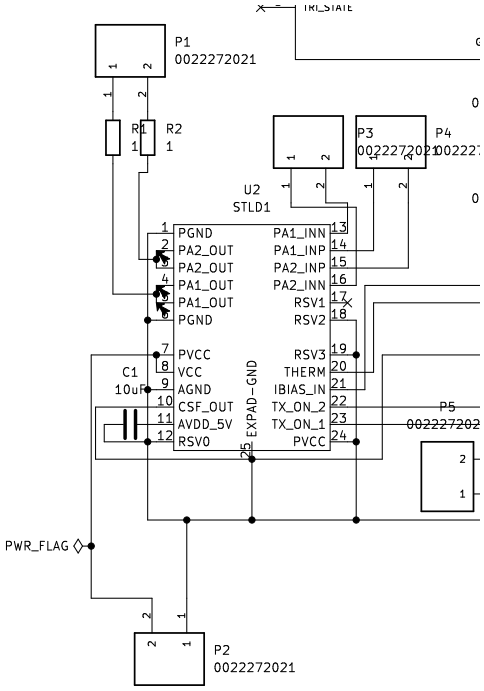

Fig. 11. **STLD1 Pre-Line Driver Schematic**

4) Miscellaneous Implementation Processes: A low power mode and a reset feature are both active low features present on the ST8500. Thus to enable use of these features, two simple switches were employed connected to these pins.

The ST8500 also requires an external 25MHz input, with voltage levels of 3.3V. A 3.3V crystal oscillator was chosen for this purpose. There is no specific model or requirements for this oscillator.

The remaining components for the main PCB consist exclusively of various pin headers for connection to external and internal features. Specifically, the I2C, SPI, JTAG (Joint Task Action Group) and GPIO ports utilise these pin headers for easy connection. Additionally, pin headers were used for any other external connections such as transmission pins, receive etc.

5) Schematic/PCB Implementation: With the component selection and general design flow for the PCB specified, the PCB schematic was designed using KiCad. The schematic for the main PCB is as shown in Fig. 12.

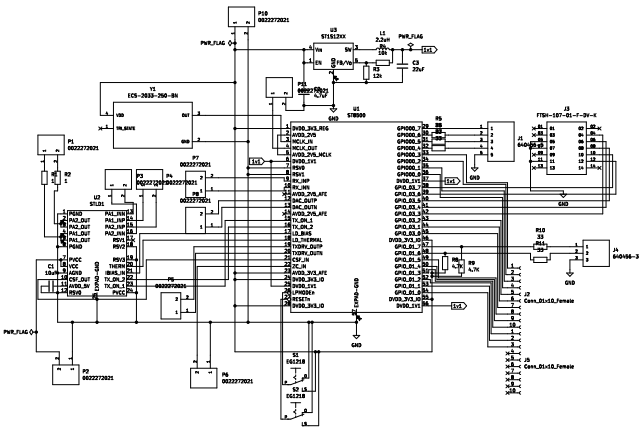

Fig. 12. **Entire Development Board Schematic**

With the schematic in place, the remaining process was to route the PCB itself, and have the PCB sent off for milling. All discrete components were manually routed, with the routing of the high pin count QFN (Quad Flat No-Lead) packages autorouted using Freerouting. After applying ground planes, and implementing vias where necessary to route the schematic, the following PCB was designed in KiCad (Fig. 13). Note that KiCad's export feature does not allow silkscreen to show over top of copper, the actual fabrication has all silkscreen text clearly visible.

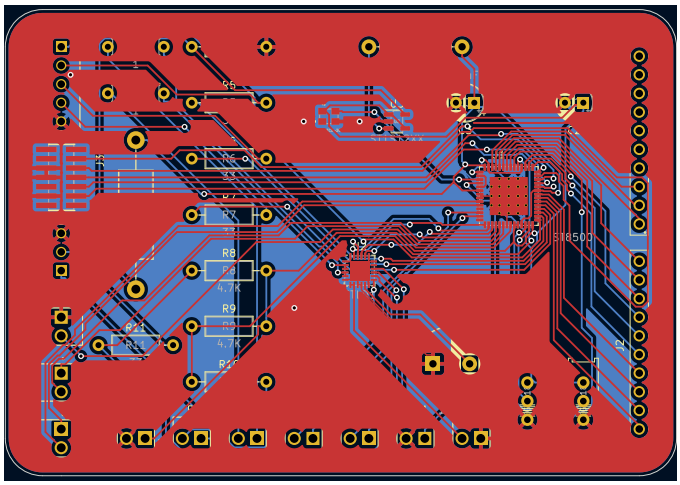

Fig. 13. **Development Board PCB Routing**

After the PCB was milled, it had to be assembled. This was an arduous process. The discrete components and pin

headers were simple to solder onto the board, but the ST8500 and STLD1 required multiple attempts to solder the extremely difficult QFN packages. The resulting PCB is as seen in Fig. 14. As you can see, two of these boards were created.

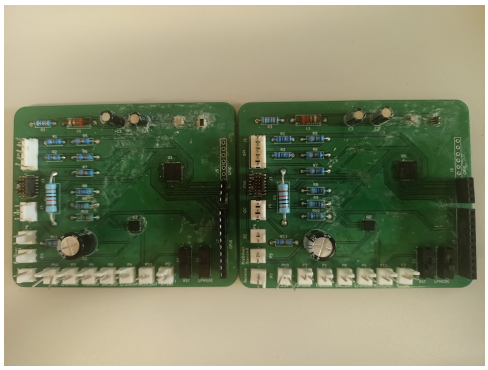

Fig. 14. **Physical Development Board PCB**

This concluded the implementation and design process of what was termed the "Development Board". The principal being that once some sort of operation was achieved with this board, a refined all in one PCB could be designed that would implement all necessary features onto a singular board. This board was never envisioned due to time constraints (this is discussed later).

E. Software Implementation Attempts

The PLC aspect of the project was not finished. After the development of both the filter system and the development board, the task of writing software/firmware for the system was not completed. However, some insight into this process was uncovered before the project end.

1) ST8500 Bootloader: The bootloader present on the ST8500 is capable of booting from an external UART host, an external SPI host and both small and large configurations of SPI flash modules [10]. Fig. 15 displays the GPIO configuration required to access each of these modes:

Boot2	Boot1	Boot0	Boot ID	Boot mode
0	0	0	0x0	Boot from UART host interface
0	0	1	0x1	Boot from SPI host interface
0	1	0	0x2	Boot from SPI external Flash (large configuration)
0	1	1	0x3	Boot from SPI external Flash (small configuration)
1	0	0	0x4	Reserved
1	0	1	0x5	Reserved
1	1	0	0x6	Reserved
1	1	1	0x7	Reserved

Fig. 15. **ST8500 Bootloader Truth Table [10]**

When booting from any of these methods, the boot process is to download and store two seperate images. The first, is the firmware image of the RTE, the second being the firmware image of the onboard ARM Cortex M4F. STMicroelectronics provides firmware images for the ST8500 based on the G3-PLC standard. These images are bundled with a library for an STM32 host interface to be able to communicate with the ST8500 via various function calls.

Although time constraints resulted in no software being executed, a general process was discovered. Writing firmware images for the ST8500 is not a useful endevour, this is because the IP (Intellectual Property) of the process to write code to generate these images is internal to STMicroelectronics and not publicly shared. As such, the first step of the process is to boot the ST8500 to the G3-PLC images provided by STMicroelectronics. The user must then leverage the ability of an STM32 microcontroller, the STM32CubeIDE developer suite, and the provided library for communication to develop code. This code once run on the STM32 can be used to operate the ST8500 in any configuration the user desires.

V. Evaluation

Evaluating the project performance in it's current state is extremely difficult. This is due to the main caveat that the project has not reached completion. Initially, the project goal was to have a bidirectional integrated PLC and VLC communication system, with a single direction standalone PLC system being considered a suitable MVP (Minimum Viable Product). In the projects current state, the MVP has not been reached, as there is a present filter system, and PCB, but no such proper operation of a PLC system. For this reason, the evaluation metrics specified in both the proposal and preliminary report must be discarded, and new metrics must be evaluated.

A. Filter System Evaluation

In order to gauge the performance of the filter system, both the individual filters and complete filter system were subjected to the same signals as the simulation, and the results compared in terms of voltage levels, and subjective noise.

1) Transmission Filter Simulated vs Physical Analysis: Fig. 16 and Fig. 17 show the frequency response and transient response at 240KHz input (signal passed) in an LTSpice simulation

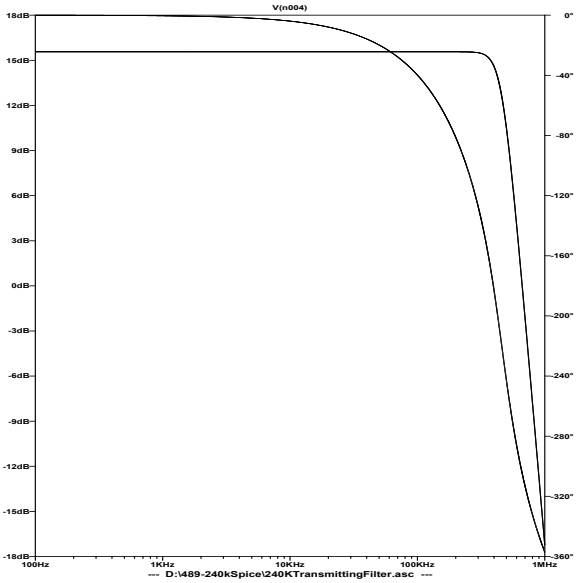

Fig. 16. **LTSpice Transmission Filter Frequency Response**

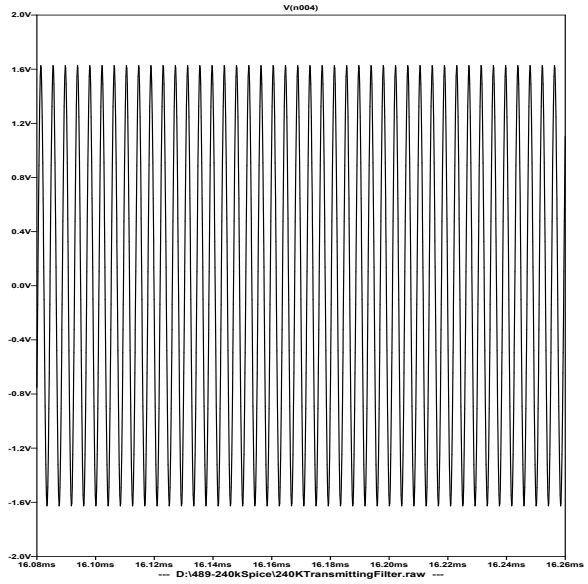

Fig. 17. **LTSpice Transmission Filter Transient Response With 240KHz Input**

Fig. 18 displays the same 240KHz input signal subjected into the physical transmission filter. Note that both the image format and size of the scope output is non changeable, as the oscilloscopes are physical devices with hardware constraints.

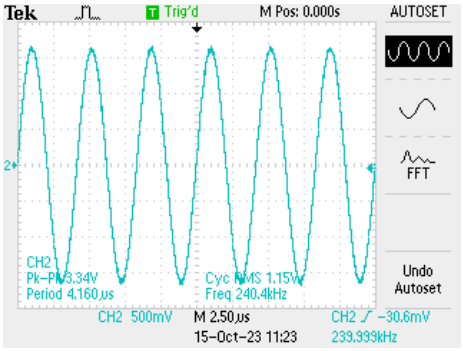

Fig. 18. **Physical Transmission Filter Oscilloscope Output With 240KHz 3.3V Input**

This filter in particular was perhaps the most successful filter in terms of physical implementation. The transmission filter successfully blocks the 1MHz high frequency signal while passing the 240KHz signal with the same voltage levels as the input. The gain in both simulation and reality are both of value 1. Additionally, the noise in the oscilloscope image is also very low, with the signal representing the input being a clean sine wave of 240KHz and 3.3V voltage level.

2) Receiving and Coupling Filter Simulated vs Physical Analysis: Fig. 19, Fig. 20, Fig. 21 and Fig. 22 show the frequency response and 240KHz transient response to both the receiving and coupling filter in an LTSpice simulation:

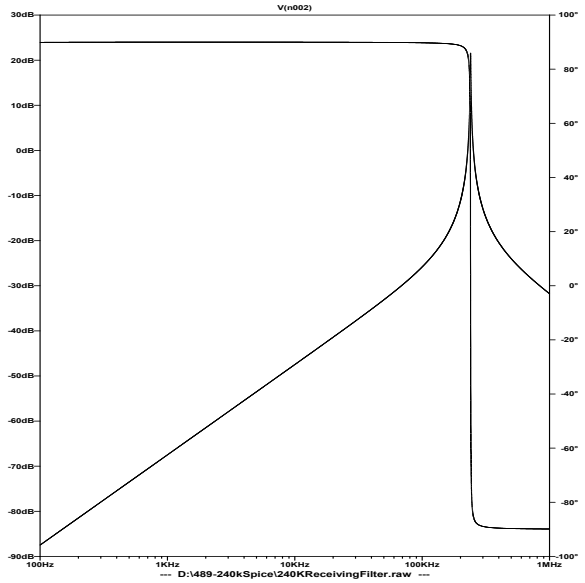

Fig. 19. **LTSpice Frequency Response Simulation of Receiving Filter**

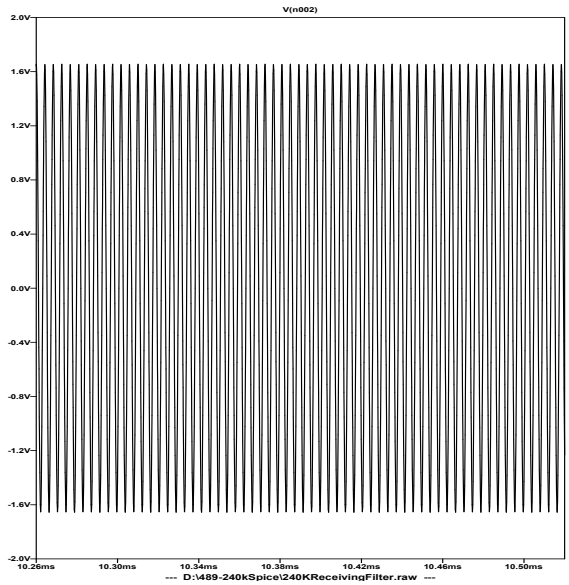

Fig. 20. **LTSpice Transient Response of Receiving Filter With 240KHz Input Signal**

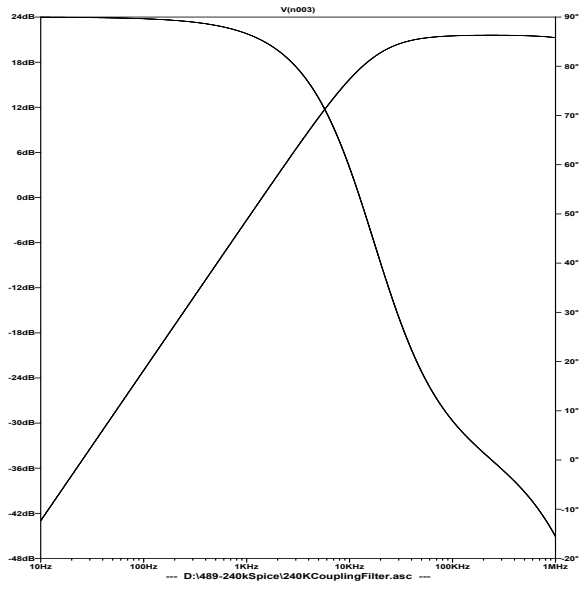

Fig. 21. **LTSpice Frequency Response Simulation of Coupling Filter**

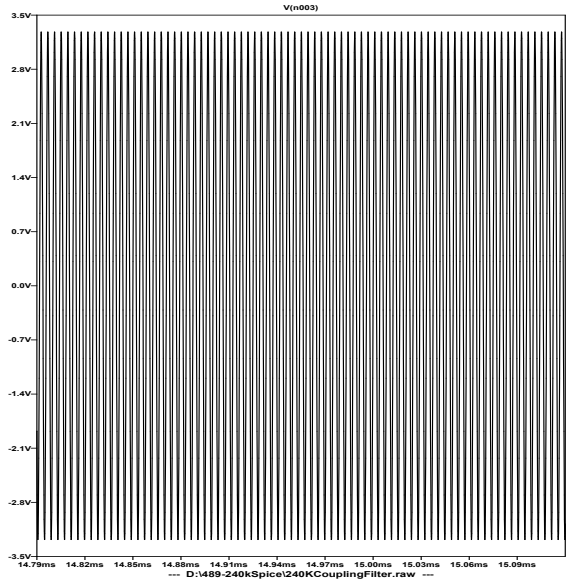

Fig. 22. **LTSpice Transient Response of Coupling Filter With 240KHz Input Signal**

It is apparent by these simulation results that the resulting physical receive and couple filter circuit board should be capable of passing a 240KHz signal while blocking a 50Hz signal. To test this, the filter was hooked up to a 50Hz 12V AC step down transformer, with a 240KHz 3.3V signal injected on top of it.

Fig. 23 displays the same 240KHz signal subjected into the physical coupling and receiving filter board.

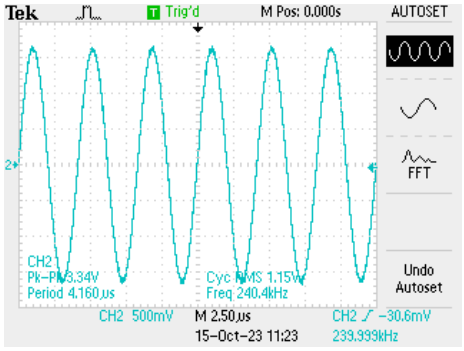

Fig. 23. **Physical Receiving and Coupling Filter Oscilloscope Output With 240KHz 3.3V Input Filtered Out From 50Hz 12V AC Mains Step Down**

The performance of these two filters into a combined system proved to be less than desirable. The output voltage level of the receiving filter given a 240KHz input at the mains end of the coupling filter was only in the range of approximately 750mV peak to peak, compared to the 3.3V input signal. However, the mains line was effectively blocked by the filter system, and the noise of the output signal is very low, showing a clean sine wave successfully received. With proper amplification, this signal should theoretically suit the needs of the PLC system well.

3) Full Filter System Simulation vs Physical Analysis + Performance at Various Distances + Filter Evaluation Conclusion: To conclude the filter evaluation, the full filter system was setup in the same theoretical setup that the final project would experience. For efficiency, the performance of the output of the full filter system was also compared at varying distances of 50Hz 12V mains line conductor.

Fig. 24 displays the output when a 240KHz 3.3V signal is injected on one end of the coupling and receiving filter to an interconnected 12V 50Hz AC line, and received on the other end. In blue is the received signal, and yellow the sent signal.

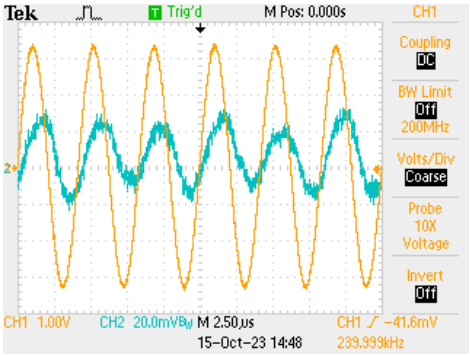

Fig. 24. **Output of Physical Full System Setup in Blue, Input Signal in Yellow**

Conversely, Fig. 25 displays these same conditions but inspected under the LTSpice simulation of schematic Fig. 26.

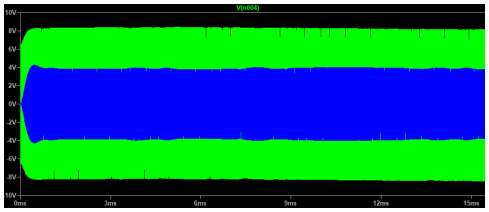

Fig. 25. **Output of Simulation Full System Setup in Blue, Input Signal in Green**

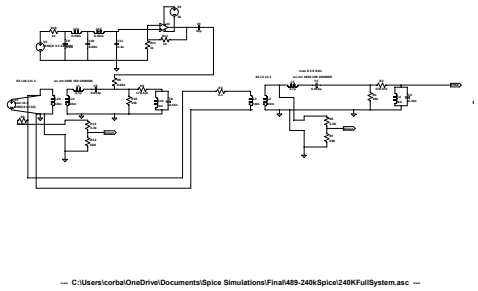

Fig. 26. **LTSpice Schematic of Full System Simulation**

From these figures, we can ascertain that the filter system in reality is not suitable for a real PLC application. The received signal is not only in the range of only a few hundred mV, but is also excessively noisy. It is possible that using the ST8500 PGA and other signal processing features that this signal could still be used to extract a full data signal, however without a functioning programmed development board, there is no conclusion that can be made on this aspect.

The final filter system evaluation is that of transmission length. To test the functional transmission length of the full filter system, the same scope results and setup that was used in Fig. 27 were again employed, but at conductor lengths of 1 meter, 3 meters and 5 meters accordingly.

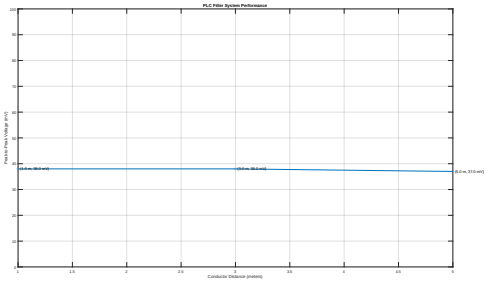

Fig. 27. **PLC Filter System Peak to Peak Voltage Output at Varying Conductor Lengths**

Although this in particular does not portray a great deal of information, it does give insight to the fact that as the mains carrier line is of a very high power, the peak to peak voltage output likely remains very similar across a large range of distances. This is backed up by the fact that narrowband PLC systems typically experience far greater range than broadband PLC systems.

4) General PCB Performance Evaluation: As the development board PCB was never made fully operational, or operational in any way other than supplying power to the board, evaluation of the board in terms of whether it satisfies the solution to the problem given is difficult. As a result, evaluation of the board is done in terms of basic expected and observed values of the voltage output of the 1.1V voltage regulator, and the 25MHz output of the crystal oscillator. Additionally, from a subjective standpoint, the development board itself theoretically contains a suitable suite of features and segments for PLC operation. That is, the board contains both a PLC modem and pre-line driver, aswell as appropriate regulators, communication protocol ports, and discrete components to ensure proper operation of the modem and it's derivatives. The areas in which this board theoretically falls short of the original specifications is that the solution is not self contained, and has no housing. It was specified originally that the final PLC system had to be self contained and have a housing. However, it is likely with further software and hardware development that this board would become capable of proper PLC operation. Fig. 28 and Fig. 29 display the output of the 25MHz crystal oscillator and the 1.1V voltage regulator.

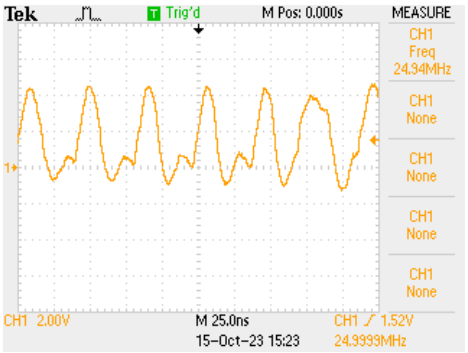

Fig. 28. **25MHz Crystal Oscillator Output**

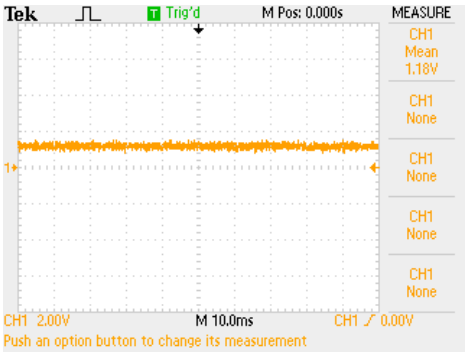

Fig. 29. **1.1V Voltage Regulator Output**

The 1.1V voltage regulator is shown to output approximately 1.18V with some noise. This is likely within tolerances

for the ST8500, but shows room for improvement in a final PCB.

The 25MHz oscillator output is shown to be of voltage levels above 4V peak to peak, with some unwanted characteristics in oscillation. However, the signal is still of approximately 25MHz frequency, and again the ST8500 likely has built in functionality for utilising this system, as the specified edge boundaries for almost all functions in the ST8500 are in the mV range.

VI. Future Work and Conclusion

It should be no surprise by this point that there is a large list of tasks required to finish the project given its unfinished nature. With this being said, there is also a small list of achievable feats given the project in its current state.

The first main future task to be completed is to create a second revision of the filter system. Although the filter system was shown to have some degree of desirable operation, the voltage levels of the signal output are small (40mV range) and plagued by excessive noise. Additionally, once this filter system was completed and verified, full operation of the development board and filter system should be established. This will involve creating software via an STM32 host controller that can interface with the given G3-PLC firmware images loaded on to the development board. As an extension to both of these tasks, a fully self contained PCB should be designed that includes all features and components required for standalone function of the PLC system.

Additionally, an enclosure for such a PCB would be desirable, as operation of a PCB in the open poses a safety risk to users.

Given the project in its current state, a student given the artefact should be able to grasp the concept of a PLC system effectively. Additionally, while the system is not operational, the skeleton for a fully operating PLC system is present, so the student should be able to bypass a large amount of the original design process.

In conclusion, the problem specified was not solved via the solution envisioned. However, this was not the cause of the solution itself, but rather the implementation of said solution. In theory, a PLC system still remains a competent and logical complimentary system to a VLC system, given its operating medium, ease of use, and relatively high speeds. Through an elaborate design process, a theoretically fully functioning PLC design was envisioned. Although via implementation the project was not finished, the project's skeleton proves a clear path forward to finish the system and create the solution envisioned.

VII. Closing Words

Thank you for Yau Hee Kho for supervising this project. While it was not complete, much was learnt in the pursuit of the design. Yau Hee Kho's careful guidance and advice was of great benefit to both the project and the learning process. It is wished for that this project is finished in the future.

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