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Practical evaluation of an interleaved boost AC-DC converter with power factor correction for a solid-state transformer

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Abstract

Solid-state transformers (SSTs) are key enabling technologies for smart grids, offering enhanced controllability, fault isolation, and active power quality improvement over conventional low-frequency transformers. Their front-end AC-DC converter must rectify grid voltage while maintaining a high power factor (PF) and low total harmonic distortion (THD). This paper presents the design, simulation, and hardware validation of a two-phase interleaved boost AC-DC PFC converter for a laboratory-scale SST, operating from 24 V AC to a regulated 48 V DC bus at approximately 100 W. A digital average-current-mode controller with interleaved 180° carriers, implemented on a TI C2000 microcontroller, regulates the DC link and shapes the input current. MATLAB/Simulink results predict approximately 89% efficiency and a well-regulated DC link, while the simulated THD and true power factor fall short of the <5% and >0.95 targets, attributed primarily to input diode-bridge conduction loss and zero-crossing distortion. A DC-bench prototype campaign confirms clean 50 kHz gate drive, correct 180° interleaving with the characteristic frequency-doubled output ripple, accurate sensing, boost operation, and a measured efficiency consistent with simulation. Because the power-factor control is an AC feature, true power factor, THD, and closed-loop regulation are reported from simulation, with full AC characterisation retained as future work. Bridgeless rectification and wide-bandgap devices are recommended to close the performance gap.

Keywords: AC-DC converter; Interleaved boost; Power factor correction; Solid-state transformer; Total harmonic distortion.

1. Introduction

The The increasing global energy demand and the transition to sustainable energy sources underscore the critical role of power electronics in modern power systems. The evolution of electrical grids into smart grids requires technologies capable of seamless energy conversion, bidirectional power flow, and advanced grid management. Within this context, the solid-state transformer (SST) is a key enabling technology. SSTs offer significant advantages over conventional low-frequency transformers (LFTs), which are typically bulky, rely on environmentally hazardous oils, and suffer from poor voltage regulation. In contrast, SSTs reduce volume and weight, isolate faults, and actively improve power quality through reactive power compensation and harmonic mitigation (Shadfar et al., 2021). A typical modular SST architecture consists of multiple cascaded power conversion stages: a front-end AC-DC rectifier, an isolated DC-DC stage, and a back-end DC-AC inverter. The front-end AC-DC stage is particularly vital, as it dictates the quality of power drawn from the grid and ensures the stability of the internal DC link upon which all subsequent conversion stages depend. Conventional rectifiers often draw distorted, non-linear currents from the utility grid, leading to poor power factor and high total harmonic distortion (THD). To mitigate these adverse effects and comply with stringent power quality standards such as IEEE 519, active power factor correction (PFC) techniques are essential (Singh et al., 2003; Rehman et al., 2022).

The selection of an appropriate AC-DC converter topology for an SST front-end involves navigating a well-documented performance-versus-practicality trade-off. The active full-bridge topology offers robust bidirectional capability but introduces shoot-through risk

and gate-drive complexity that is disproportionate to its performance benefit in a modular, low-voltage context. The totem-pole bridgeless boost converter achieves very high theoretical efficiency. However, its dependence on wide-bandgap semiconductors for viable continuous conduction mode (CCM) operation — due to the reverse recovery characteristics of silicon MOSFET body diodes, and its associated gate-drive complexity present significant practical barriers for a robust laboratory implementation. These limitations are consistent with findings from a recent systematic review of PFC converter topologies, which explicitly rates the totem-pole topology as high complexity and identifies GaN or SiC devices as a prerequisite for realising its full performance potential (Quiroga et al., 2025).

The interleaved boost converter addresses these implementation challenges directly. This topology employs multiple parallel shift-commutated boost stages operating with a fixed phase offset — typically 180° for a two-phase configuration — which induces a ripple cancellation effect at the input (Jang and Jovanović, 2007). This significantly reduces the size requirements for electromagnetic interference (EMI) filters and passive components, a critical advantage for the compact modular construction of an SST (Quiroga et al., 2025). Distributing current between parallel branches also lowers per-device conduction losses and thermal stress, resolving primary hardware reliability concerns in compact SST modules. Critically, each individual boost stage uses a simple high-side/low-side gate drive circuit with no shoot-through risk — a significant practical advantage over both the full-bridge and totem-pole alternatives. Hardware-validated studies confirm that the interleaved boost consistently achieves power factors above 0.99 and efficiencies above 95% using mature silicon devices and standard average-current-mode control (Quiroga et al., 2025; Singh et al., 2023). The topology is therefore well-suited to serve as a robust, reproducible foundational module in a laboratory-scale SST.

Despite these established advantages, the existing literature does not provide a dedicated experimental characterisation of the interleaved boost topology specifically in the role of a low-voltage SST front-end module. Published studies on interleaved boost converters are predominantly focused on standalone performance at fixed operating points, or on high-power EV charging applications where power levels, device technologies, and design priorities differ substantially from those of a modular SST context. The performance metrics most critical to SST integration — namely, DC bus voltage stability under dynamic loading, current balance between interleaved phases, and efficiency across a realistic partial-load range — are not comprehensively evaluated in the current literature for this specific application. This paper addresses that gap directly by providing a rigorous, data-rich experimental evaluation of an interleaved boost PFC converter designed and characterised as a laboratory-scale SST front-end module.

1.1. Objective of the paper

This paper investigates the design, control, and practical implementation of a two-phase interleaved boost AC-DC converter for a laboratory-scale SST. In particular, the research addresses three questions:

- How effectively does the interleaved boost topology reduce input current ripple and THD compared to a mathematically equivalent single-stage converter?
- What design trade-offs arise in tuning an average-current-mode control scheme — a single current loop with two 180°-interleaved pulse width modulation (PWM) carriers — to maintain branch current sharing and a stable DC link under load variation?

- Can the implemented prototype reliably achieve a conversion efficiency greater than 80% and a power factor above 0.95 across typical SST load conditions?

2. Literature review

This section synthesises the peer-reviewed literature on AC-DC converters for solid-state transformer (SST) front-end applications and establishes the technical context for the topology selected in this study. A systematic review of literature published between 2020 and 2025, accessed through IEEE Xplore, Scopus, and Web of Science, was organised into four themes: converter topologies and topology selection; control strategies and architectures; semiconductor device technologies; and modular architectures and system integration for SSTs. The review maps established performance benchmarks and, in doing so, exposes the specific gap that the three research questions in Section 1.1 are designed to address.

2.1. Converter topologies and topology selection

The circuit topology determines both the theoretical efficiency of a converter and the practical burden of implementing it. The recent literature shows a consistent trend toward increasing integration, specialisation, and complexity in pursuit of higher efficiency and power density. Multilevel topologies, including the packed U-cell and flying-capacitor resonant converters, are frequently investigated for their power-quality advantages (Cardoso et al., 2023; Peter and Mathew, 2021), while the demands of electric-vehicle (EV) charging have driven research into high-gain buck-boost stages and single-phase isolated bidirectional converters for vehicle-to-grid operation (Singh et al., 2023; Di et al., 2023). A recent PRISMA-based systematic review of PFC converter topologies by Quiroga et al. (2025) surveys six major topology families and characterises the interleaved boost as a high-efficiency variant of the boost family with only average control complexity — a favourable position relative to the totem-pole bridgeless converter, which it rates as very-high efficiency but high complexity and identifies as dependent on GaN or SiC devices to realise its potential.

Two topologies were initially adopted as candidates for the SST front-end in this study before practical implementation experience prompted a revision. The active full-bridge (H-bridge) converter was attractive for its bidirectional capability and well-understood control architecture. In practice, however, the four-switch configuration introduced a persistent risk of shoot-through, and ensuring precisely matched dead-time across all switching transitions while simultaneously enforcing PFC current shaping imposed a gate-drive burden disproportionate to the performance benefit for a foundational laboratory module. Its higher conduction losses relative to bridgeless alternatives further reduced its appeal. This experience reflects an analytical gap noted in the literature: the full-bridge is well documented as a topology, but its specific implementation challenges in a low-voltage modular SST context are not rigorously characterised (Ortiz-Castrillon et al., 2021).

The totem-pole bridgeless boost converter is the most intensively researched PFC topology in the recent literature, owing to its exceptional theoretical efficiency when implemented with wide-bandgap (WBG) semiconductors; reported peak efficiencies exceed 93—97% in boundary- and continuous-conduction modes respectively (Gurudiwan et al., 2024; Shahzad et al., 2022). This performance, however, carries a significant practical cost. The reverse-recovery behaviour of the body diode in the slow-leg MOSFETs during continuous conduction mode (CCM) — the preferred mode for this study's power level and switching frequency — causes severe switching losses in silicon

devices and renders the topology effectively incompatible with silicon MOSFETs in CCM. While GaN devices eliminate this problem, their cost, limited availability, and the additional gate-drive complexity they demand presented prohibitive barriers for a robust, replicable laboratory module (Huang and Huang, 2017). Quiroga et al. (2025) corroborate this assessment, noting that hardware implementations of the totem-pole topology consistently operate at kilowatt power levels with GaN or SiC devices — a context far removed from the low-voltage, silicon-based module targeted here.

Following this assessment, the interleaved boost PFC converter was selected as the most appropriate topology for the study. The interleaved boost phase-shifts two or more standard boost stages — typically by 180° for a two-phase configuration — across a shared DC output bus, and offers several well-documented practical advantages. The interleaving principle produces substantial input current ripple cancellation, reducing the RMS current through the input EMI filter and permitting a reduction in filter component size that is valuable for the compact construction of an SST module (Safayatullah et al., 2022). The current stress on each inductor and switch is reduced because each phase carries only a fraction of the total input current, which lowers conduction losses and eases thermal management (Manoj et al., 2023). Most importantly for this application, each boost stage requires only a simple high-side/low-side gate drive with no shoot-through path, which is markedly more robust to implement than the four-switch protection of the H-bridge or the body-diode management of the totem-pole. Reported performance is well characterised: with silicon MOSFETs at switching frequencies of 50—100 kHz, peak efficiencies above 95% are consistently achieved, extending above 97% with SiC devices, alongside power factors above 0.99 and THD below 5% using standard average-current-mode control (Singh et al., 2023; Quiroga et al., 2025). The topology therefore trades the theoretical efficiency ceiling of the totem-pole for a more predictable, reproducible performance profile — a trade-off that is central to this study and defines its contribution.

Table 1. Comparison of representative AC-DC converter topologies for SSTs

Topology	Key advantage	Key limitation	Efficiency potential	Application suitability
Interleaved boost (selected)	Input ripple cancellation; reduced per-device current stress; simple, shoot-through-free gate drive	Higher component count than single-phase boost; inductors must be well matched	High (>95% Si; >97% SiC)	Robust modular SST front-end (this study)
Active full-bridge (H-bridge)	Bidirectional power flow; well-understood control	Shoot-through risk; gate-drive complexity; higher conduction loss	Moderate—high (~95—97%)	Considered; revised in early design
Totem-pole bridgeless boost	Very high theoretical efficiency; low conduction loss	Body-diode reverse recovery in CCM; requires GaN/SiC	Very high (>98% GaN)	Considered; rejected on practical grounds
Vienna / 3-level T-type	Unity PF; low THD; high power density	Requires DC-link capacitors; voltage balancing	High (~99% interleaved)	High-power EV chargers, V2G
Swiss / buck-type	High efficiency; inherent step-down	Unidirectional by default; current-handling challenge	High (~99% SiC)	EV battery charging, DC distribution
Matrix (isolated bidirectional)	Compact; no electrolytic capacitors; high PF	High control complexity	High (~97.8%)	Bidirectional charging, V2G

2.2. Control strategies and architectures

The control strategies reported for AC-DC converters are increasingly diverse, with a clear trend toward adaptive, modular, and reconfigurable schemes. Sophisticated control for EV charging is prominent — adaptive neuro-fuzzy inference systems are applied to two-stage bidirectional chargers (Seth and Singh, 2021), and coordinated control of modular multilevel converters integrates charging stations into complex networks (Wang and Liu, 2023). At the converter level, modulation strategies that exploit discontinuous conduction mode improve the efficiency of bidirectional converters (Passalacqua et al., 2021). For the interleaved boost specifically, the control architecture is mature and directly applicable to a digital implementation (Zhang et al., 2004): average-current-mode control (ACMC), in which an outer voltage loop shapes a rectified-sine current reference and an inner current loop drives the input current to track it, provides high line-current quality and robust DC-link regulation (Dixon, 1990), with phase interleaving enforced simply by offsetting the PWM carriers. Quiroga et al. (2025) confirm that hardware-validated implementations using PI, proportional-resonant, and pulse-frequency-modulation control all achieve power factors at or above 0.99, and identify the standard PI controller as sufficient for high power factor in boost-type PFC converters. This breadth of validated options allows the controller to be matched to the available digital platform without compromising the target performance, and frames the second research question: the trade-offs involved in tuning such a scheme to maintain branch current sharing while holding a stable DC link.

2.3. Semiconductor device technologies

The literature underscores the central role of semiconductor technology in converter performance, reliability, and efficiency, with attention to device-level loss balancing for converter longevity (Qiu et al., 2021), intelligent gate drivers for condition monitoring (Sundararajan et al., 2022), and the strong coupling between topology choice and device stress (Domino et al., 2023). For the interleaved boost, device selection is considerably simpler than for the rejected candidates: standard silicon MOSFETs with low-reverse-recovery diodes, or with SiC Schottky boost diodes, are sufficient to meet the target benchmarks, in direct contrast to the totem-pole's dependence on GaN or SiC for viable CCM operation. Quiroga et al. (2025) note that the faster switching and lower losses of WBG devices are most justified in demanding, high-power applications; for a laboratory-scale SST front-end prioritising robust, reproducible operation over maximum power density, mature silicon technology remains the practical and economical choice, with the additional benefit of a large body of established gate-drive reference designs.

2.4. Modular architectures and system integration for SSTs

The SST literature reframes the front-end AC-DC stage not as a standalone device but as an integrated module within a larger cascade. Modular designs are favoured for the scalability and robustness they confer: the semi-modular three-phase AC/DC structure of Dao et al. (2022) reduces component count and removes the need for high-speed communication through decentralised control, while modular multilevel converter-based SSTs maintain DC-bus stability under complex loads (Zheng et al., 2022). Reviews of SST-based microgrid architectures emphasise that system partitioning and control flexibility are critical to overall stability (Chalbi and Boukettaya, 2021), and advanced schemes such as partial power processing and inductive ripple filtering further improve integration efficiency (Zheng et al., 2023; Teng et al., 2022). This system-level perspective directly reinforces the topology selection: a stable, well-regulated DC bus for the downstream DC-DC stage places a premium on predictable, well-characterised performance, and the inherent ripple cancellation, implementation simplicity, and control maturity of the

interleaved boost align closely with the reliability and longevity requirements of a modular SST building block.

Across the four themes, the literature is rich in highly specialised standalone converters and in high-level reviews of complete SST systems, but it does not provide a dedicated experimental characterisation of the interleaved boost topology in the specific role of a low-voltage SST front-end module. The metrics most critical to SST integration — DC-bus voltage stability under dynamic loading, current balance between interleaved phases, and efficiency across a realistic partial-load range — remain uncharacterised for this application. This study addresses that gap through the rigorous design, implementation, and experimental evaluation set out in the research questions of Section 1.1: the reduction in input current ripple and THD relative to an equivalent single-stage converter; the design trade-offs in tuning the average-current-mode controller for branch-current sharing and DC-link stability; and the achievable efficiency and power factor across typical SST load conditions.

3. Research methods

The research followed a phased and iterative methodology, progressing from theoretical design through simulation validation to physical prototype construction and experimental characterisation. Each phase informed the next, with simulation results guiding hardware decisions and hardware observations feeding back into the analytical framework. The five phases — converter design and component selection, simulation and optimisation, prototype construction, experimental validation, and data analysis — are described in the sub-sections below.

3.1. Converter design and component selection

The interleaved boost PFC converter was designed to accept a single-phase AC input and produce a regulated DC bus voltage, with the following target specifications: input voltage 24 V AC (rms) at 50 Hz, DC bus output voltage 48 V DC, rated output power approximately 100 W (a 23 Ω resistive load), switching frequency 50 kHz, target efficiency greater than 80%, power factor above 0.95, and input current THD below 5%. These targets were selected to be consistent with the performance benchmarks established in the literature review and to represent a meaningful and achievable specification for a laboratory-scale SST front-end module. The complete design and the selected components are summarised in Table 2.

The power stage comprises a single-phase full-bridge diode rectifier (D1—D4) feeding a two-phase interleaved boost stage that shares a common DC output bus. Each boost leg consists of a 220 µH inductor, a low-side MOSFET switch, and a boost diode, with the two legs driven by PWM signals held at a fixed 180° phase offset. Component sizing proceeded analytically for each element as follows.

The boost inductor for each phase was sized to maintain continuous conduction mode (CCM) across the operating range, with an acceptable peak-to-peak ripple current. The minimum inductance per phase is given by:

$$L = V_{dc} \cdot (V_{pk} - V_{in}(t)) \,/\, (\Delta I_L \cdot f_{sw}) \qquad (1)$$

where V_{dc} is the DC bus voltage, V_{pk} is the peak input AC voltage, $V_{in}(t)$ is the instantaneous input voltage, ΔI_L is the desired peak-to-peak inductor current ripple per phase, and f_{sw} is the switching frequency. A standard 220 µH power inductor (Bourns 1140-221K-RC) was

selected for each leg. At the rectified peak (V_{pk} ≈ 34 V, V_{dc} = 48 V, duty ≈ 0.29) and f_{sw} = 50 kHz, this gives a calculated per-leg peak-to-peak ripple of approximately 0.9 A, maintaining continuous conduction mode over the bulk of the line cycle.

Table 2. Converter design summary and key components

Parameter / Component	Value / Part
Input voltage	24 V AC (rms), 50 Hz
DC bus output voltage	48 V DC
Rated output power	~100 W (23 Ω resistive load)
Switching frequency	50 kHz
Topology	Single-phase diode-bridge rectifier + two-phase interleaved boost
Boost inductors (L1, L2)	220 µH, 7.4 A, 50 mΩ DCR each (Bourns 1140-221K-RC)
DC-link capacitor (C1)	2200 µF, 63 V electrolytic (Nichicon UVZ1J222MHD)
Bridge and boost diodes (D1—D6)	MBR10100G (100 V, 10 A Schottky)
Power MOSFETs (Q1, Q2)	IPP048N12N3G (120 V, 4.8 mΩ R_o, TO-220)
Gate driver (U1)	UCC27524ADR (dual, non-isolated, low-side)
Phase current sensing	0.02 Ω shunt (WSL2512R0200FEA) + INA180A1 amplifier, per leg
Output voltage sensing	47 kΩ / 3.3 kΩ divider (ratio 0.066)
Inrush / protection	10 Ω NTC inrush limiter (TDK B57235S0609M051) + 5 A fuse
Digital controller	TI LAUNCHXL-F2800137 (C2000, F280013x)

The DC-link capacitor was sized to limit the output voltage ripple to an acceptable level under full load, using:

$$C_{dc} = P_{out} / (2 \cdot \omega \cdot V_{dc,avg} \cdot \Delta V_{dc,ripple}) \quad (2)$$

where P_{out} is the maximum output power, ω is 2π times the input AC frequency (2π × 50 rad/s for a 50 Hz supply), $V_{dc,avg}$ is the average DC link voltage, and $\Delta V_{dc,ripple}$ is the allowable peak-to-peak ripple on the DC bus. A 2200 µF electrolytic capacitor (C1) was selected, which holds the simulated bus ripple to within approximately 4.15 V peak-to-peak (±2 V) at full load.

The MOSFET switches were selected based on voltage rating (must exceed V_{dc} with adequate margin), current rating (must handle peak inductor current per phase), and on-state resistance RDS(on) to minimise conduction losses. The conduction loss per device is:

$$P_{cond} = I_{rms}^2 \cdot R_{DS(on)} \quad (3)$$

The switching loss per device is approximated by:

$$P_{sw} \approx ½ \cdot V_{DS} \cdot I_D \cdot (t_{on} + t_{off}) \cdot f_{sw} \quad (4)$$

The power MOSFETs (Q1, Q2) are Infineon IPP048N12N3G devices, rated 120 V with a typical on-state resistance of 4.8 mΩ in a TO-220 package. The 120 V rating provides a wide margin over the 48 V bus, and the low RDS(on) minimises conduction loss. Silicon MOSFETs were selected in preference to GaN or SiC devices, consistent with the design rationale: the interleaved topology achieves its target performance with mature silicon

technology, which eliminates the gate-drive complexity and cost associated with wide-bandgap semiconductors at this power level. The switches are driven by a single non-isolated dual gate driver (Texas Instruments UCC27524ADR) through 10 Ω gate resistors; because both boost switches are low-side referenced to the common ground, no gate-drive isolation is required.

Schottky diodes (MBR10100G, rated 100 V and 10 A) were used throughout, both for the input rectifier bridge (D1—D4) and for the boost diodes (D5, D6). The choice of Schottky devices for the boost position directly realises the low-reverse-recovery requirement identified in Section 2.3, avoiding the recovery losses that would arise with standard silicon diodes. Inductor copper and core losses were estimated using:

$$P_L = I_{rms}^2 \cdot R_{DCR} + P_{core} \quad (5)$$

where R_{DCR} is the DC winding resistance and Pcore represents frequency-dependent core losses estimated from the core manufacturer's datasheet. Thermal management was addressed through heat sink selection for the MOSFET devices, with junction-to-ambient temperature rise calculated as:

$$\Delta T = P_{diss} \cdot R_{th} \quad (6)$$

to confirm that device junction temperatures remained within safe operating limits at full load.

Voltage sensing was implemented using resistive divider networks, and phase current sensing using shunt resistors:

$$V_{sensed} = V_{actual} \cdot R_2 / (R_1 + R_2) \quad (7)$$

$$V_{shunt} = I_{actual} \cdot R_{shunt} \quad (8)$$

The output voltage was sensed through a resistive divider (R3 = 47 kΩ, R4 = 3.3 kΩ), giving a scaling ratio of 0.066 so that the 48 V bus maps to approximately 3.15 V at the 3.3 V ADC input. Each leg current was sensed across a 0.02 Ω precision shunt (Vishay WSL2512R0200FEA) using a current-sense amplifier (Texas Instruments INA180A1, gain 20 V/V), providing independent per-leg current feedback to the controller.

The complete converter, comprising the input protection and rectifier stage, the two interleaved boost legs, the gate-drive circuit, and the voltage- and current-sensing networks, is shown in the schematic of Figure 1.

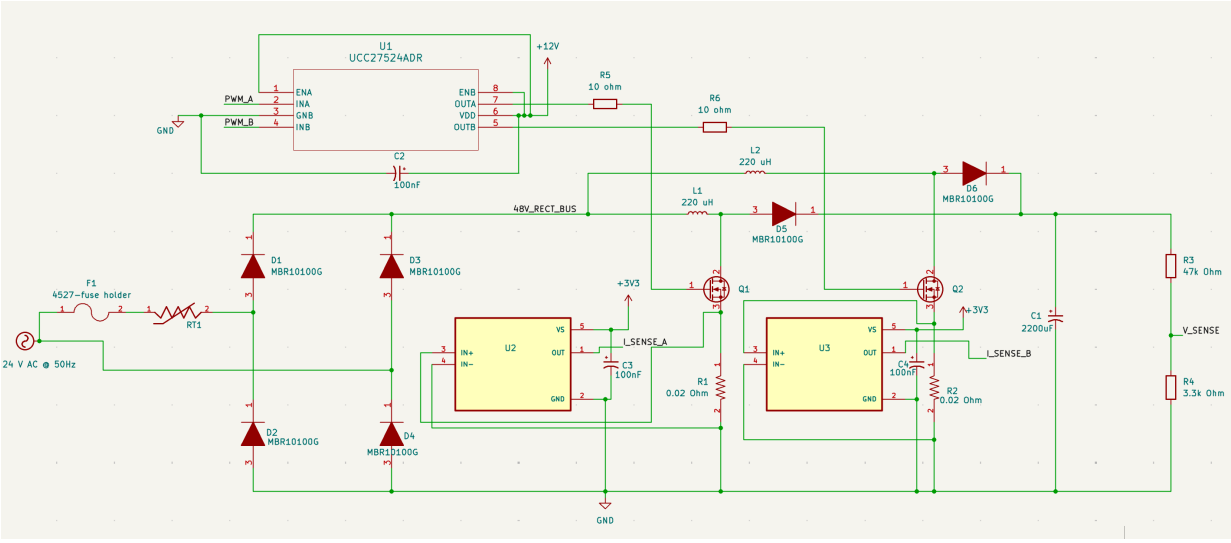

Figure 1. Power-stage and sensing schematic of the two-phase interleaved boost PFC converter, showing the input rectifier (D1–D4), the two interleaved boost legs (L1/Q1/D5 and L2/Q2/D6), the shared 2200 µF DC-link capacitor, the dual gate driver (U1), and the voltage- and current-sensing networks

3.2. Simulation and optimisation

Prior to and alongside hardware construction, the complete converter design was modelled in MATLAB/Simulink with Simscape Electrical, using a fixed-step solver at a 1 µs step (twenty steps per switching period). The two PI control loops were implemented in discrete time at a 20 µs sample period with back-calculation anti-windup. In the model the boost MOSFETs were treated as ideal switches (no conduction or switching loss) and the inductors as lossless, while the diodes carried a 0.8 V forward drop; the consequences of this idealisation for the loss budget and for the interpretation of the simulated efficiency are addressed in Section 4.1. The model was used to predict efficiency, input power factor, THD, DC bus voltage regulation, and per-leg behaviour, and to confirm correct interleaved operation of the two boost legs before committing to hardware.

The control scheme was a digital average-current-mode controller. An outer voltage loop compared the measured DC bus voltage against the 48 V reference and produced a current-amplitude command; this command multiplied a rectified-sine template (generated as the absolute value of a 50 Hz sinusoid) to form the input current reference, enforcing a sinusoidal current drawn in phase with the rectified input. A single inner current loop drove the total measured inductor current to track this reference, and its output was compared against two triangular carriers held 180° apart to generate the two gate signals (duty1, duty2); the complete control scheme is shown in Figure 2. Branch-current sharing therefore relied on the matched 220 µH inductors and the symmetric carriers rather than on active per-leg regulation — a deliberate simplification whose consequences are examined in Section 4. Each loop used a discrete-time PI controller of the form:

$$u(k) = K_p \cdot e(k) + K_i \cdot \Sigma e(j) \cdot T_s \qquad (9)$$

where K_p is the proportional gain, Ki is the integral gain, e(k) is the tracking error at time step k, and T_s is the sampling period. The voltage loop was tuned to Kp = 0.1, Ki = 3 (output clamped to the range 0—7), and the current loop to K_p = 0.05, Ki = 3 (output clamped to

0—1). Within the stable range, the converter showed limited sensitivity to the current-loop gains — a behaviour discussed in Section 4.2, where it is linked to the structural, rather than tuning-limited, origin of the observed distortion.

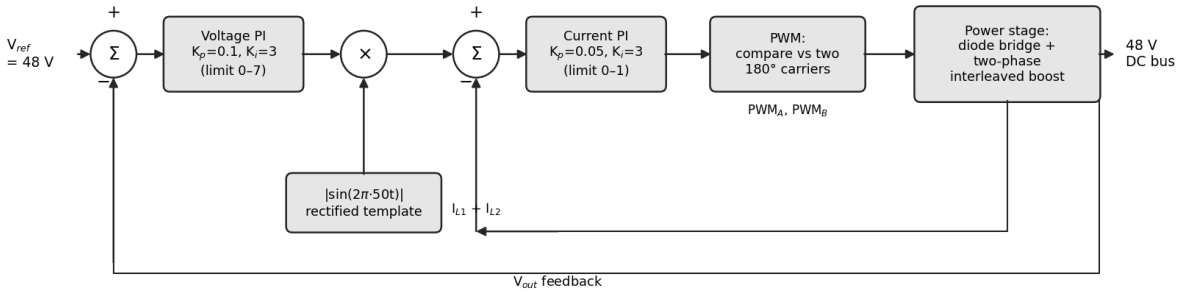

Figure 2. Average-current-mode control scheme with 180° interleaved carriers

The key simulation performance metrics captured were efficiency, power factor, and input current THD, defined as:

$$\eta = P_{out} / P_{in} \times 100\% \quad (10)$$

$$PF = P_{in} / (V_{in,rms} \cdot I_{in,rms}) \quad (11)$$

$$THD_I = \sqrt{(I_{in,rms}^2 - I_{in,fund,rms}^2)} / I_{in,fund,rms} \times 100\% \quad (12)$$

where $I_{in,rms}$ is the total RMS input current and $I_{in,fund,rms}$ is the RMS value of the fundamental component. Power factor was evaluated in two ways: a displacement power factor obtained from the instantaneous real and reactive power (the cosine of the phase angle), and a true power factor that additionally accounts for distortion via the input current THD. The distinction is material here, because the two diverge substantially when THD is high, as reported in Section 4.2. A single-leg equivalent boost converter — identical component values and control but with the second leg disabled — was also simulated to compare input current ripple directly against the two-leg configuration, addressing the first research question. The simulation results are presented and discussed in Section 4.

3.3. Prototype construction and test methodology

A laboratory-scale prototype was constructed on a two-layer printed circuit board, laid out in KiCad with attention to high-frequency current-path minimisation, thermal dissipation, and reduction of parasitic inductance around the MOSFET switching nodes. The board was commercially fabricated and hand-populated with the components of Table 2. During bring-up, a localised region in which the copper pour and a track had not transferred correctly was repaired by drilling through and adding underside jumper wires; this rework is noted here for transparency, as the added wire length introduces a small, asymmetric parasitic that is a candidate contributor to any per-leg current imbalance observed in testing. The populated prototype is shown in Figure 3; the annotated KiCad schematic of Figure 1, the board layout, and the complete Simulink model are provided in the Supplementary Material.

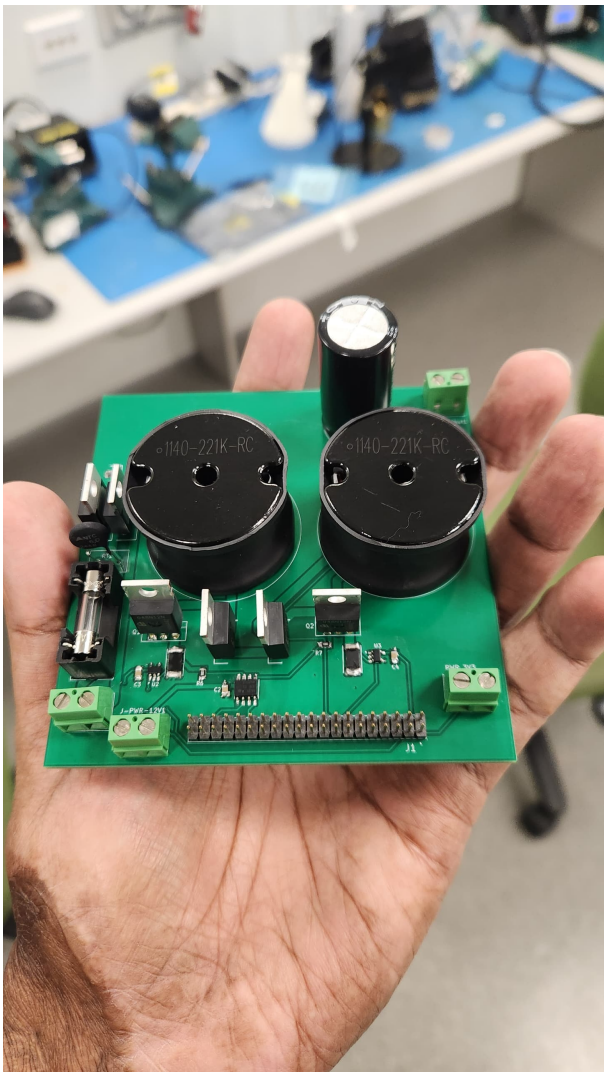

Figure 3. Populated two-phase interleaved boost PFC

The digital control algorithm was implemented on a Texas Instruments LAUNCHXL-F2800137 (C2000, F280013x target) development board, which connects to the power board through a 40-pin header. The C2000 enhanced PWM (ePWM) peripheral generates the two 180°-offset gate signals with hardware-controlled carrier phase and dead-time, while on-chip ADC channels sample the output voltage and both leg currents. The use of the ePWM peripheral, rather than the sawtooth-and-comparator scheme used in simulation, is expected to give cleaner and more consistent gate timing in hardware, which is relevant to the ripple-cancellation discussion in Section 4.4.

The experimental test bench is summarised in Table 3. Within the testing window the converter was driven from a DC bench supply rather than an AC source (see Section 4.6): a dual bench DC supply provided the 12 V gate-driver rail and a variable boost input, a TENMA 72-13210 electronic load set the output power in constant-current mode, and waveform capture used a Tektronix TPS2024 oscilloscope (four isolated channels, 200 MHz) with a Tektronix P2220 voltage probe; no current probe was available. Input and output power were computed from the supply and load readings, and switching and ripple waveforms were recorded on the oscilloscope.

Table 3. Experimental test bench equipment

Instrument	Model	Role / key specification
Controller	TI LAUNCHXL-F2800137 (F280013x)	Runs the control firmware; ePWM gate signals and ADC sensing
DC supply	Dual bench DC supply	12 V gate-driver rail and variable boost input
Electronic load	TENMA 72-13210 (300 W, 120 V, 30 A)	Constant-current DC load
Oscilloscope	Tektronix TPS2024 (+ P2220 probe)	4-channel, 200 MHz, isolated; no current probe available

Steady-state performance is to be measured at four load levels at 25%, 50%, 75%, and 100% of rated output power — at nominal input voltage, with efficiency calculated from the ratio of measured output to input power and power factor and THD recorded at each point. Input current ripple is to be measured at the rectified peak and compared between two-leg and single-leg operation to quantify the interleaving benefit, addressing the first research question. Dynamic performance is to be assessed by applying step load changes and recording the DC bus transient response (overshoot, undershoot, and settling time to within ±2% of steady state), addressing the second research question, and robustness is to be checked at ±10% input voltage. As an AC source was not available within the testing window, hardware validation was performed using a DC input to characterise the boost power stage and the digital control loop; the AC-dependent metrics — true power factor and input-current THD — are reported from simulation, with full AC characterisation retained as future work. The DC measurement campaign and its results are presented in Section 4.6.

4. Results and discussion

This section presents the simulation results for the interleaved boost PFC converter (Sections 4.1–4.5), followed by the DC-bench hardware validation (Section 4.6), evaluating both against the three research questions of Section 1.1 and the design targets of Section 3.1. The headline simulation metrics are collected in Table 4.

4.1. Conversion efficiency and loss mechanisms

At the nominal 100 W operating point the converter drew 112.8 W from the source and delivered 100.1 W to the load, giving a conversion efficiency of 88.7%, which meets the 80% efficiency target adopted in Section 3.1. Because the model treats the boost MOSFETs as ideal and the inductors as lossless (Section 3.2), the entire 12.7 W difference between input and output is attributable to diode conduction: the four bridge-rectifier diodes and the two boost diodes, each carrying a 0.8 V forward drop. This makes the loss budget exact rather than estimated — with no other lossy elements present, diode conduction accounts for the whole of the simulated loss, as set out in Table 5.

Table 4. Summary of simulated performance at the nominal operating point (24 V AC, 48 V DC, ~100 W, 50 kHz)

Metric	Simulated value	Target	Status
Input power	112.8 W	—	—
Output power	100.1 W	~100 W	Met
Efficiency	88.7%	>80%	Met
Fundamental input current	6.43 A	—	—
Input current THD	38.3%	<5%	Not met
Displacement PF	0.999	—	Phase only
True power factor	0.93	>0.95	Shortfall
DC bus voltage (avg)	≈48 V	48 V regulated	Met
DC bus ripple (100 Hz)	4.15 V pk-pk (≈8.6%)	—	—
Two-leg input ripple	1.19 A pk-pk	—	See Section 4.4
Single-leg input ripple	0.97 A pk-pk	—	Comparison inconclusive
Operating duty cycle	≈0.3 at rectified peak (≈0.31–0.63 over the line cycle)	—	—

Table 5. Modelled loss budget at the 100 W operating point

Element	Modelled drop	Average loss
Bridge rectifier diodes (×4)	Vf = 0.8 V	conduction
Boost diodes (×2)	Vf = 0.8 V	conduction
Boost MOSFETs (×2)	ideal (Vf = 0)	0 W
Inductors (×2)	ideal (R = 0)	0 W
Total diode conduction		≈ 12.7 W
Measured total loss (Pin − Pout)		≈ 12.7 W

The dominance of diode conduction is significant in two ways. First, it is precisely the loss mechanism that the bridgeless and totem-pole topologies reviewed in Section 2 are designed to eliminate, and which this study deliberately accepted in exchange for the implementation robustness of a diode-bridge front end; the bridge rectifier, carrying the full input-side current through two series diodes at every instant, is the larger contributor. Second, and importantly for interpreting the figure, the 88.7% is an optimistic bound: the real prototype will additionally incur MOSFET conduction and switching loss, inductor copper and core loss, and sensing and capacitor ESR loss, none of which are present in the idealised model. The measured hardware efficiency should therefore be expected to fall somewhat below the simulated value, and the hardware measurement remains the authoritative test. In answer to the third research question, the efficiency target was met in simulation, the loss is shown to be diode-dominated, and bridgeless rectification is identified as the single most effective route to higher efficiency in future work.

Efficiency was evaluated across the output-power range rather than at the rated point alone. Figure 4 plots the simulated load sweep of Section 4.5 together with the measured DC-bench points of Section 4.6. The simulated efficiency remained between 87.0% and

88.7% from 50 W to 100 W, showing that conversion performance is essentially flat over the upper half of the operating range rather than optimised at a single point. The measured points lie 3–4 percentage points lower and span only the 10–30 W range reachable on the DC bench; they rise from 82.4% to a plateau near 85%, the characteristic light-load behaviour of fixed semiconductor voltage drops forming a diminishing fraction of the throughput as load increases. The two data sets are not directly comparable — the simulated points are closed-loop at rated AC input, the measured points open-loop on a DC input — and are plotted together to show the trend of each rather than to imply a like-for-like comparison.

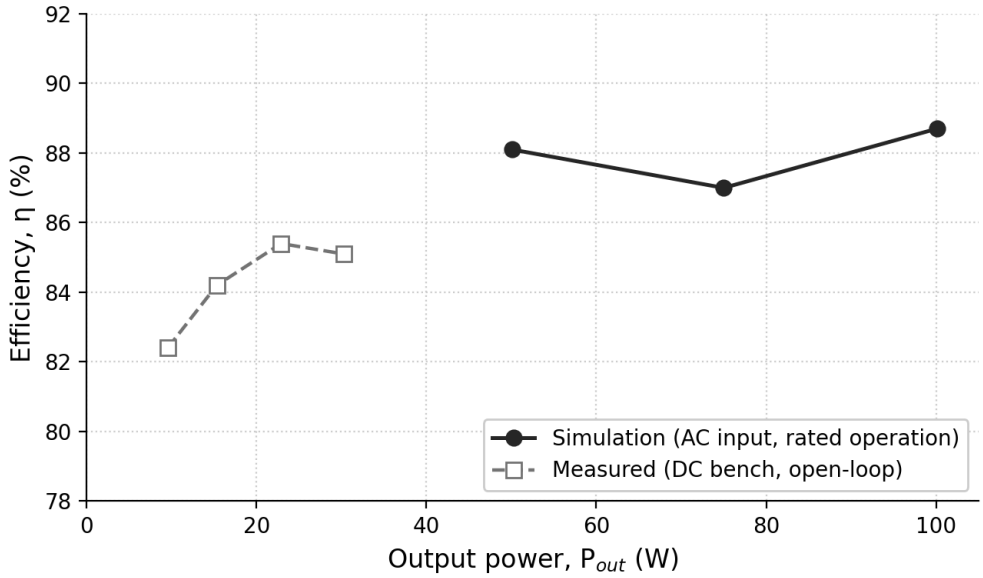

Figure 4. Conversion efficiency against output power. Simulated points (closed-loop, 24 V AC input) are shown alongside the measured DC-bench points (open-loop, 20 V DC input); the two are different operating modes and are plotted together to show the trend of each

4.2. Power factor and harmonic distortion

The displacement power factor was essentially unity (0.999), but this figure reflects only the phase relationship between the fundamental components and substantially overstates the quality of the drawn current. The true power factor, which incorporates distortion, was 0.93 — below the 0.95 target — and the simulated input current THD was 38.3%, far above the 5% target, against a fundamental input current of 6.43 A. The harmonic content was dominated by the third harmonic at 150 Hz (approximately 33.5% of the fundamental), with smaller seventh (approximately 8.7%) and ninth (approximately 4.2%) components. Figure 5 shows the input voltage and current in steady state: the current broadly follows the sinusoidal voltage, confirming that power factor correction is acting, but with clear distortion near the zero crossings. Figure 6 shows the corresponding harmonic spectrum.

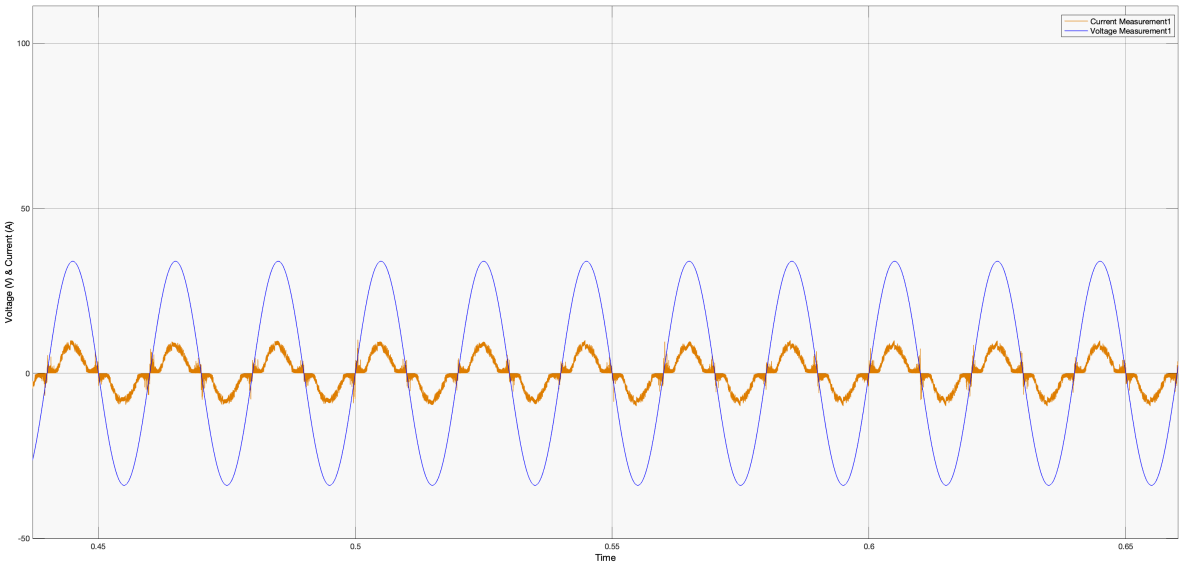

Figure 5. Input voltage (blue) and input current (yellow) in steady state

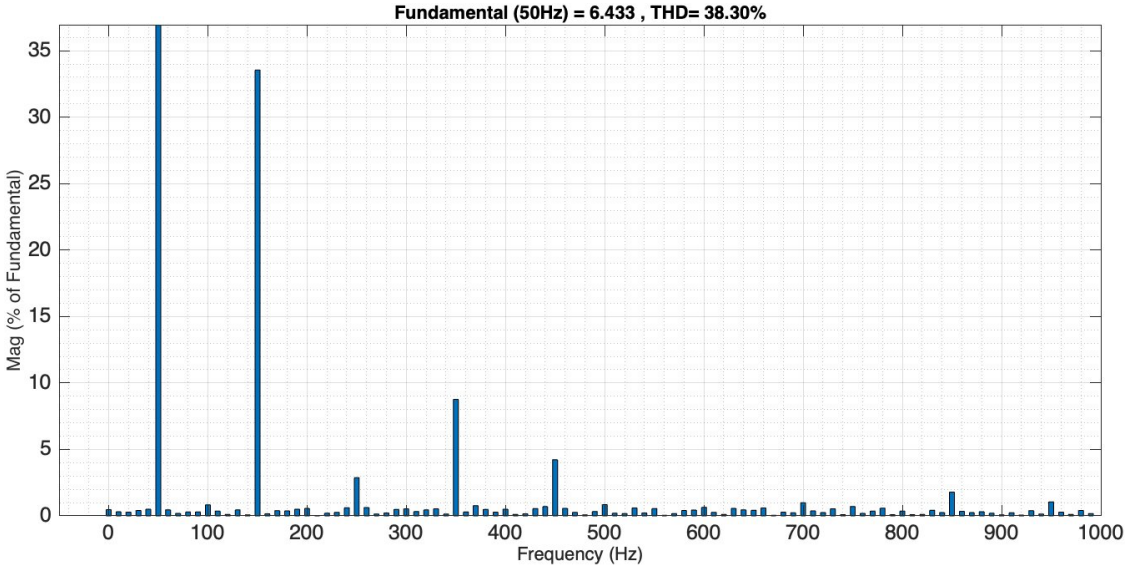

Figure 6. Harmonic spectrum of the input current (THD = 38.3%, dominant third harmonic)

The third-harmonic dominance is the characteristic signature of zero-crossing distortion: near the AC zero crossings the input voltage approaches zero, the boost stage briefly loses controllability, and the current fails to track its sinusoidal reference (García et al., 2003). This effect is aggravated by the modest boost ratio of this design (48 V from a 34 V rectified peak, a ratio of about 1.4) and by the limited bandwidth of the single current loop relative to the rectified reference it must follow.

The behaviour of the control signal itself supports this interpretation. Figure 7 shows the simulated duty command produced by the current loop over five rectified half-cycles. The command varied at the 100 Hz rectified-line rate between approximately 0.31 and 0.63 and remained within the linear modulation range throughout, never reaching the 0–1 clamp limits. The broad minima near 0.31 coincide with the rectified voltage peaks and agree with the theoretical duty of D = 1 − Vin/Vout ≈ 0.29 obtained for a 34 V rectified

peak and a 48 V bus, confirming the operating duty reported in Table 4. Between these minima the command rose toward the zero crossings, where the falling instantaneous input voltage demands greater boost, but reached only about 0.63 rather than approaching unity, because the rectified-sine current reference collapses toward zero over the same interval. The sharp transient reductions visible at the crossings are the control-signal expression of the loss of controllability described above, and provide independent evidence that the third-harmonic distortion originates in the topology and the reference shape rather than in the choice of loop gains.

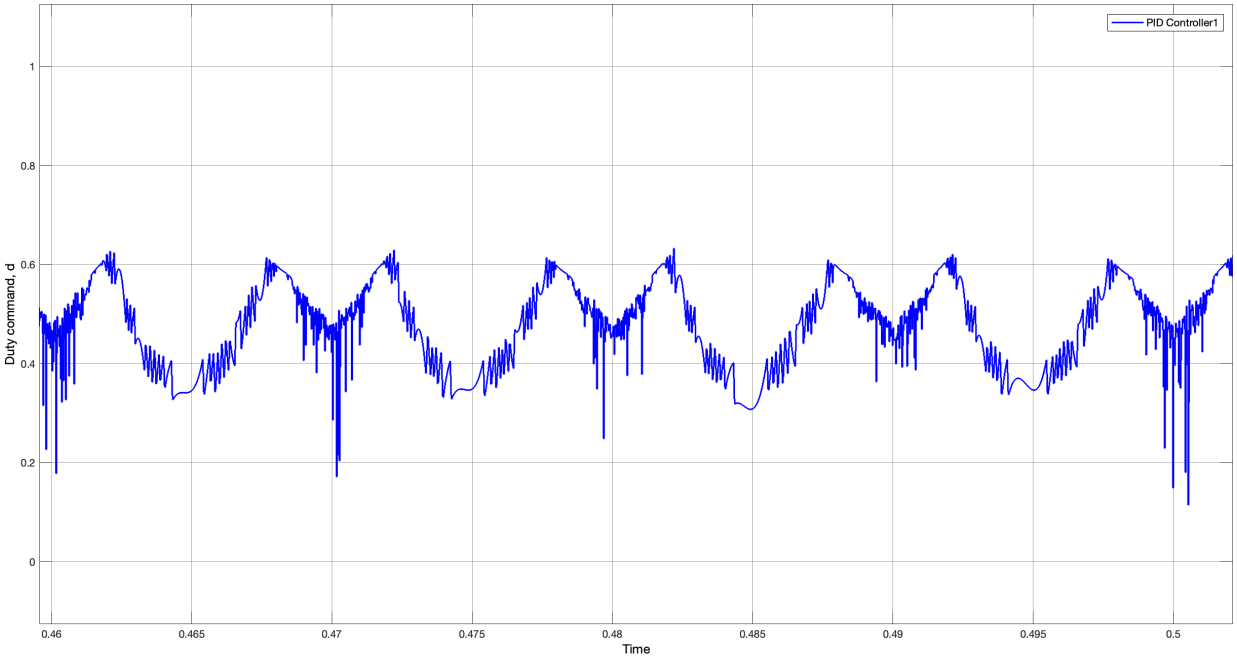

Figure 7. Simulated duty command from the inner current loop over five rectified half-cycles. The command follows the 100 Hz rectified-line envelope between approximately 0.31 and 0.63, remaining within the linear modulation range; the transient reductions coincide with the input-voltage zero crossings

In answer to the third research question, the power-factor and THD targets were not met in simulation, with input-current distortion identified as the limiting factor; input-voltage feedforward and a higher current-loop bandwidth in the hardware implementation, and ultimately a bridgeless front end, are the indicated remedies.

4.3. DC-link regulation and control behaviour

The control scheme regulated the output well, holding the DC bus in the region of 48 V with a low-frequency (approximately 100 Hz) ripple of about 4.15 V peak-to-peak (approximately 8.6%), the characteristic double-line-frequency ripple of a single-phase PFC stage (Zhu and Pratt, 2009), as shown in Figure 8. This is the clearest success of the implementation and is directly relevant to the SST context, where the front-end converter must present a stable DC link to the downstream DC-DC stage. In answer to the second research question, the single voltage-and-current-loop scheme with interleaved carriers achieved stable DC-link regulation; the principal trade-off it embodies is that, by acting on the summed current rather than regulating each leg independently, it provides no active correction of branch-current imbalance. Sharing between the two legs therefore depends on the matched 220 µH inductors and symmetric carriers, and is sensitive to component tolerance and to layout asymmetry such as the hand-rework described in Section 3.3. The

hardware measurements in Section 4.6 quantify this imbalance at approximately 15–20%.

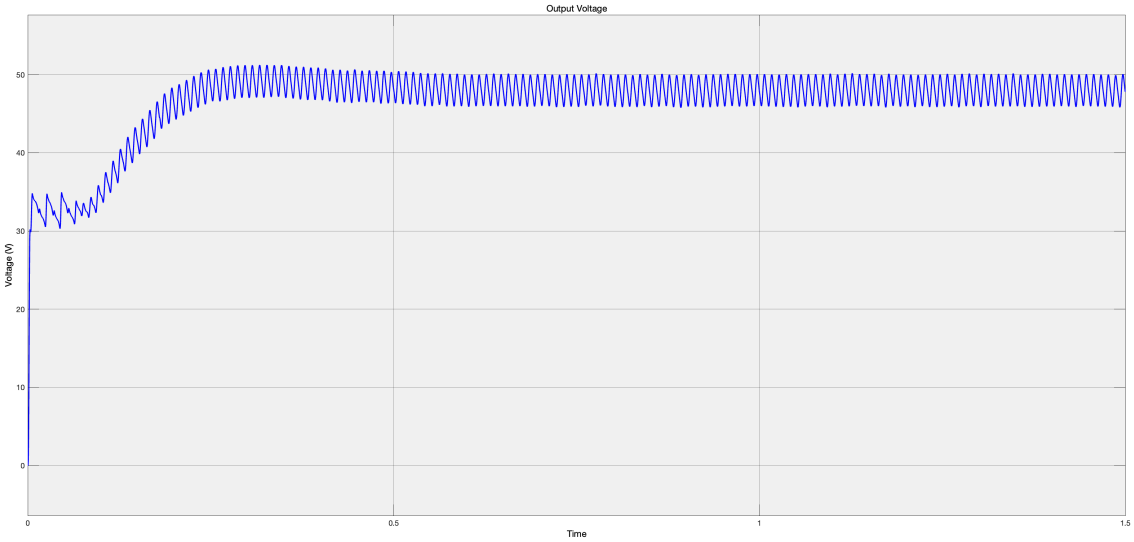

Figure 8. DC output voltage during start-up and steady state, showing regulation near 48V

4.4. Interleaving and input current ripple

Interleaved operation was examined by comparing the individual inductor-leg currents and the total input current. As shown in Figure 9, the two leg currents operated with an approximate 180° phase offset, the current rise of one leg coinciding with the fall of the other, confirming that the interleaving scheme functions correctly at the per-leg level. The corresponding gate-drive signals (provided in the Supplementary Material) show the second leg offset by approximately half a switching period, with an on-time of roughly one third of the 20 µs switching period, consistent with the operating duty of approximately 0.3 at the rectified peak.

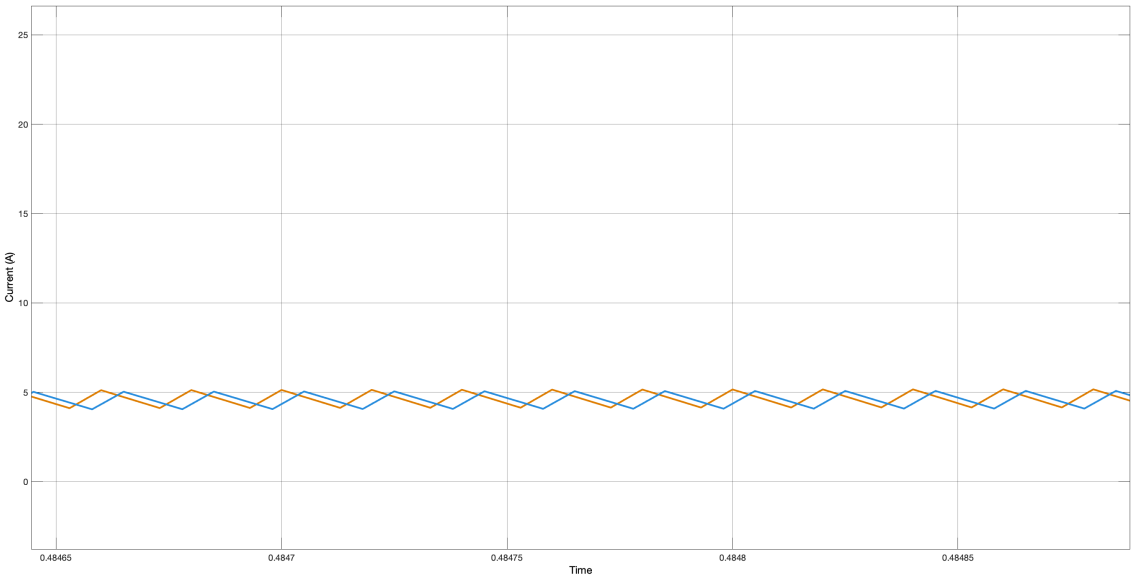

Figure 9. Inductor-leg currents showing 180° interleaved operation

The total input current switching ripple, measured at the peak of the rectified half-cycle where it is most pronounced, was approximately 1.19 A peak-to-peak with both legs active, and approximately 0.97 A with the second leg disabled at the same total power; these are shown in Figures 10 and 11.

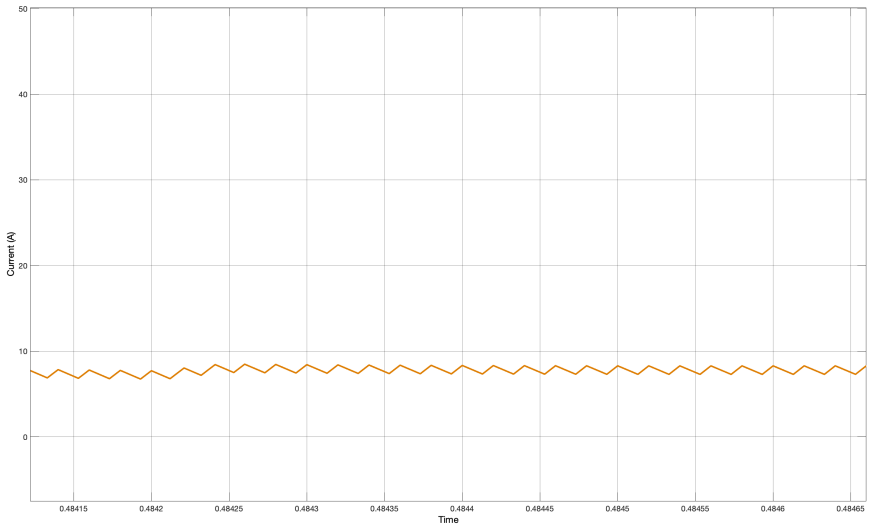

Figure 10. Total input current ripple, single-leg operation (envelope peak)

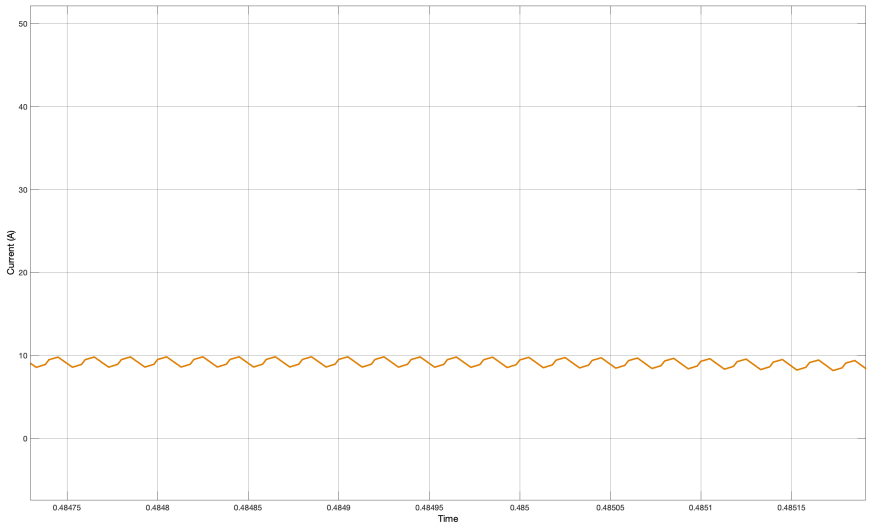

Figure 11. Total input current ripple, two-leg interleaved operation (envelope peak)

The theoretical expectation is that two-leg operation should exhibit lower total ripple than single-leg operation, owing to partial cancellation of the two legs' ripple currents. The simulation did not clearly reproduce this reduction: the two magnitudes were small and of comparable order, and their difference fell within the cycle-to-cycle variation of the current waveform, so the net ripple-cancellation benefit could not be quantified reliably from the simulation alone. Several factors are likely to have contributed. The current loop was tuned conservatively for stability, permitting cycle-to-cycle variation comparable in magnitude to the switching ripple and partially masking the cancellation. The converter also operates at a duty cycle of approximately 0.3, well away from the 0.5 point at which interleaving cancellation is greatest (Jang and Jovanović, 2007), so even

under ideal control the theoretical cancellation here is only partial. Finally, the simulated PWM was generated with a sawtooth-and-comparator scheme rather than a dedicated peripheral, which may introduce small timing inconsistencies between the legs. In answer to the first research question, interleaving was confirmed to operate correctly, but the expected net ripple reduction could not be demonstrated in simulation; its quantification is deferred to the hardware, where the C2000 ePWM peripheral provides precise carrier phasing and is expected to yield a cleaner comparison.

4.5. Operating-range performance

A load sweep at the baseline gains (24 V AC) was completed at 100%, 75%, and 50% load, and an input-voltage sweep at ±10% (21.6 V and 26.4 V AC) at full load. The results are collected in Table 6.

Table 6. Simulated performance across load and input-voltage sweeps

Vin (V AC)	Load	Pout (W)	Pin (W)	Eff (%)	THD (%)	True PF	Stable?
24	100%	100.1	112.8	88.7	38.3	0.93	Yes
24	75%	75.0	86.2	87.0	44.4	0.91	Yes
24	50%	50.1	56.8	88.1	see note	see note	Yes
24	25%	—	—	—	—	—	Diverged*
21.6	100%	100.1	112.9	88.6	34.9	0.94	Yes
26.4	100%	100.4	110.5	90.8	41.8	0.92	Yes

As the load is reduced, efficiency stays high and roughly flat (88.7% at full load, 87.0% at 75%, 88.1% at 50%) and the output remains regulated near 48 V, confirming that the converter holds its conversion performance and regulation across the operating range. The input current THD, however, worsens as load falls, rising from 38.3% at full load to 44.4% at 75% load. This is expected behaviour for a boost PFC stage: at lighter loads the fundamental input current shrinks while the fixed distortion sources (the conduction dead-zone of the diode bridge near the mains zero crossings, and switching-frequency content) remain roughly constant in absolute terms, so the ratio that defines THD rises. At 50% load this effect becomes severe enough that the reported THD exceeds 200% with a broadband spectrum; the percentage is then an artefact of the small fundamental rather than a genuine waveform-quality measure, and is reported qualitatively ("metric breaks down; spectrum broadband") while efficiency, regulation, and displacement power factor remain well behaved.

At 25% load the simulation did not reach a stable steady state: the output voltage diverged rather than settling, reaching non-physical values. This was investigated rather than discarded — the solver was already fixed-step at 1 µs, and both PI loops had correct saturation limits with active anti-windup — and is identified as a numerical convergence limit of the averaged-reference control model at very light load, where the small commanded current and slow capacitor dynamics interact poorly with the fixed-step discrete solver. It is therefore a limitation of the simulation, not a predicted behaviour of the physical converter (marked * in Table 6). The validated simulation range accordingly extends to approximately 50% load, and light-load behaviour is more appropriately characterised on the hardware.

Across the input-voltage sweep, the trends are physically consistent. As the input voltage rises, the current required to deliver 100 W falls (fundamental input current 7.36 A, 6.43 A, and 5.65 A at 21.6 V, 24 V, and 26.4 V respectively); because the dominant loss is current-dependent diode conduction, this lower current improves efficiency at higher input voltage (88.6%, 88.7%, 90.8%). The THD moves in the opposite direction, rising modestly with input voltage (34.9%, 38.3%, 41.8%), consistent with the reduced boost ratio and lower conduction angle. The output remained regulated near 48 V and the converter was stable at all three points, confirming that the control loop maintains regulation across the specified ±10% input tolerance, with efficiency and distortion trading off in the expected directions.

4.6. Hardware validation (DC bench)

Hardware validation was carried out on a DC bench. As an AC source was not available within the testing window, a DC input was used to characterise the boost power stage and the digital control loop: a DC source passes through the input rectifier and exercises the boost, the interleaving, the sensing and ADC chain, and the PWM exactly as the rectified portion of an AC input would. The two AC-dependent metrics — true power factor and input-current THD — are properties of the AC input-current waveform and cannot be produced from a DC operating point; they are therefore reported from simulation (Section 4.2), with full AC characterisation retained as future work. The equipment used is listed in Table 3.

Gate-drive verification confirmed clean operation of both legs. The gate signals swing 0–12 V at 50 kHz with the two legs offset by half a switching period, and the captured frequency of 50.0145 kHz (Figure 12) confirms the target after the ePWM timer-period configuration was set. This gate-drive pass is the precondition for all subsequent power-on testing.

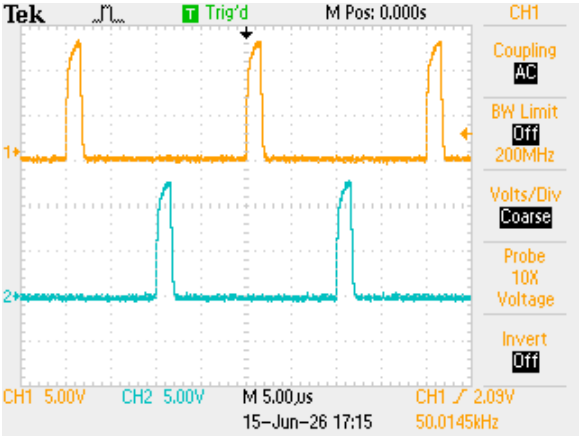

Figure 12. Measured gate drive of the two legs at 10% duty — interleaved 50 kHz square waves 180° apart (50.0145 kHz)

With the auxiliary rails verified, the sensing chain was checked against bench references. The output-voltage divider ratio measured a consistent 0.0656, matching the 3.3 kΩ/(47 kΩ + 3.3 kΩ) design value, so the controller's reported bus voltage is trustworthy; the two per-leg current-sense outputs tracked the load current at the designed 0.4 V/A scaling and were balanced at the lighter operating points. In an open-loop duty sweep at 10 V input, the output followed the boost relation $V_{out} \approx V_{in}/(1-D)$ — for example, 13.27 V

measured at 50% duty against a 13.4 V multimeter cross-check — confirming correct boost operation of both legs.

The interleaving benefit was confirmed directly. Figures 13 and 14 show the two per-leg current-sense signals conducting alternately, half a switching period apart, and their summed waveform; Figure 15 shows the output-voltage ripple, whose dominant component lies at 100 kHz — exactly twice the 50 kHz switching frequency. This frequency-doubling is the measured signature of two-phase interleaving and is the hardware counterpart to the ripple-cancellation behaviour examined in simulation (Section 4.4), providing experimental evidence for the first research question. One measurement limitation should be noted: each shunt conducts only during its own MOSFET on-time, so Figures 13 and 14 show the on-time portion of each leg current rather than the full continuous inductor triangle; a current probe on an inductor lead, which was not available, would show the complete waveform.

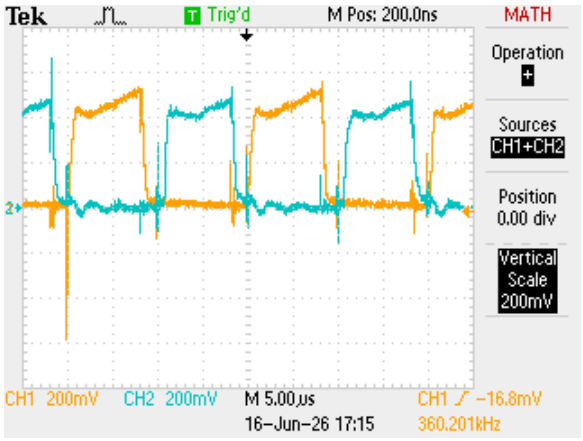

Figure 13. Measured per-leg current-sense signals conducting half a switching period apart — direct evidence of 180° interleaving

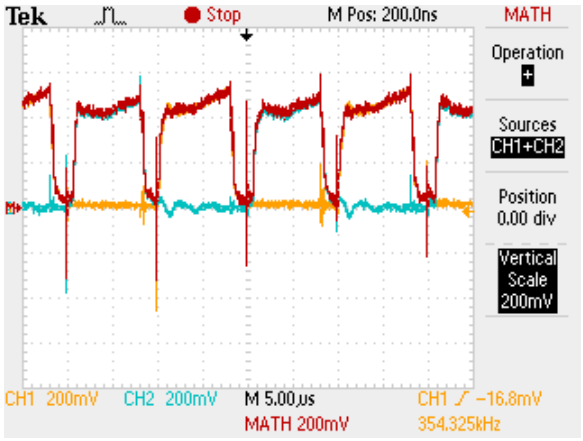

Figure 14. The two leg currents with the scope Math channel showing their sum (the combined input draw)

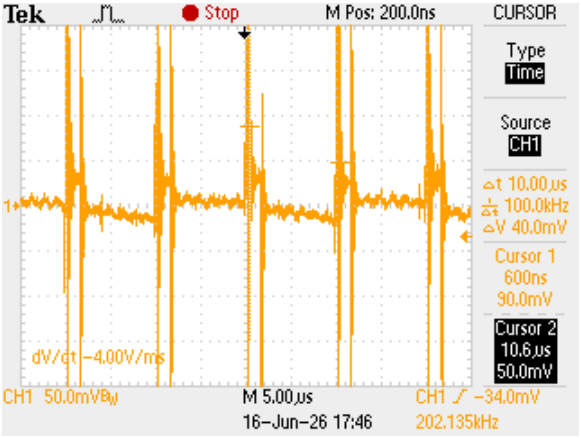

Figure 15. Measured output-voltage ripple; cursors give 10.00 µs (100.0 kHz), twice the 50 kHz switching frequency — the frequency-doubling signature of interleaving

Converter efficiency was measured in an open-loop DC load sweep at a representative 20 V input and fixed 50% duty (Table 7). Measured efficiency rose from 82.4% at light load to a peak of approximately 85% near 0.75 A. This is consistent with the 88.7% simulation figure once the losses omitted by the idealised model — MOSFET conduction and switching, inductor copper, and the sensing and inrush elements — are taken into account, and it confirms the diode-dominated loss picture of Section 4.1. The lower efficiency seen at a 10 V operating point reflects the fixed semiconductor and inrush-limiter voltage drops forming a larger fraction of a small input, rather than a property of the converter at its rated point.

Table 7. Measured open-loop DC efficiency (20 V input, fixed 50% duty)

Iout (A)	Vin (V)	Iin (A)	Vout (V)	Pin (W)	Pout (W)	Eff (%)
0.25	20	0.58	38.22	11.60	9.56	82.4
0.50	20	0.91	30.65	18.20	15.33	84.2
0.75	20	1.34	30.53	26.80	22.90	85.4
1.00	20	1.78	30.29	35.60	30.29	85.1

Closed-loop regulation was attempted on the DC bench. Because the controller implements sinusoidal current-shaping for power-factor correction — an AC-operation feature — it could not regulate a DC output: the synthesised rectified-sine reference commands boosting only near the notional sine peaks and backs off near the zero crossings, holding the effective average duty below that required to reach the voltage target, so the output rose slowly and plateaued near 18–20 V while the voltage-loop integrator wound up against this structural limit. Closed-loop regulation is validated in simulation (Section 4.3); full closed-loop hardware validation requires the AC source and is identified as future work.

Several findings from prototype bring-up inform the interpretation of these results. An inter-leg current imbalance of approximately 15–20% was measured, consistent with component and shunt tolerances on a hand-assembled prototype and with the absence of active per-leg current balancing in the implemented control (Section 3.2). The transition from discontinuous to continuous conduction was observed as the light-load output settling from an elevated value toward the loaded operating point as load increased beyond roughly 0.5 A. Finally, because the input and output do not share a common ground — they are separated by the rectifier bridge — the input voltage was measured

from the floating supply rather than referenced to board ground; this is a measurement constraint of the topology rather than a circuit fault, and is noted for reproducibility.

4.7. Synthesis

Taken together, the simulation establishes a converter that meets its output-power, efficiency, and DC-link-stability goals while falling short on power factor and THD, and the DC hardware campaign corroborates the core of this picture. The power-quality shortfalls are coherently explained by two mechanisms: the conduction loss of the input diode bridge, and zero-crossing current distortion under a conservatively tuned single current loop. Both are consistent with the literature and with the design's stated priorities — the diode-bridge loss is the known cost of a bridge front end that bridgeless topologies remove, and which this study accepted in exchange for robustness. The DC measurements confirm correct gate drive, interleaving, sensing, and boost operation, with a measured efficiency consistent with the idealised model once real device losses are included. Two caveats bound the simulation evidence: the idealised device models make the 88.7% efficiency an optimistic upper bound, consistent with the lower measured DC efficiency of Section 4.6; and the model loses numerical validity below approximately 50% load. The AC-dependent power-quality metrics and closed-loop regulation accordingly remain to be confirmed on an AC source.

5. Conclusion and recommendations

This paper set out to design, simulate, build, and characterise a two-phase interleaved boost AC-DC converter with power factor correction as a foundational front-end module for a laboratory-scale solid-state transformer, operating from 24 V AC to a regulated 48 V DC bus at approximately 100 W. The interleaved boost was selected over the active full-bridge and totem-pole bridgeless alternatives on the grounds of implementation robustness, after first-hand design experience confirmed the practical barriers of those topologies. Against the three research questions, the study found that interleaving operates correctly: simulation showed the two legs 180° out of phase, and DC-bench measurements confirmed it directly through the characteristic 100 kHz (double-switching-frequency) output ripple, although the full magnitude of input-ripple cancellation awaits a current-probe measurement under AC (first question). The single average-current-mode loop with interleaved carriers regulated a stable 48 V DC link in simulation, with the implementation trade-off that branch-current sharing is passive; a measured inter-leg imbalance of 15–20% on the prototype is consistent with this and with hand-assembly tolerances (second question). The simulated efficiency (88.7%) met the 80% target and was corroborated by a measured DC efficiency peaking near 85%, while the simulated true power factor (0.93) and input-current THD fell short of the 0.95 and 5% targets, with input diode-bridge conduction loss and zero-crossing distortion identified as the dominant limiters (third question). The principal contribution is a documented, reproducible design supported by DC hardware validation, with the AC-dependent power-quality metrics and closed-loop regulation established in simulation and identified for full hardware validation as future work.

5.1. Recommendations

With DC bring-up and characterisation complete, the immediate priority is AC-input testing using a mains-frequency source to obtain the measured power factor and THD and to validate closed-loop voltage regulation, which the DC bench could not exercise because of the converter's power-factor current-shaping — together with a current-probe measurement to quantify the input-ripple-cancellation magnitude directly. To improve performance in a future revision, three directions are indicated. First, replacing the input

diode bridge with a bridgeless or semi-bridgeless front end (Huber et al., 2008; Chen et al., 2020) would remove the single largest efficiency loss identified in Section 4.1, accepting the additional gate-drive complexity discussed in Section 2. Second, the input-current distortion could be reduced by increasing the current-loop bandwidth and adding feedforward of the rectified input voltage to suppress zero-crossing distortion, and by adding active per-leg current balancing to make branch sharing independent of component matching. Third, adopting wide-bandgap (SiC or GaN) devices would permit higher switching frequency and lower switching loss, improving power density. Finally, a targeted sensitivity study of THD against current-loop gain and of ripple cancellation against duty ratio would confirm the structural origin of the distortion proposed in Section 4 and is recommended as a low-cost addition to the analysis.

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